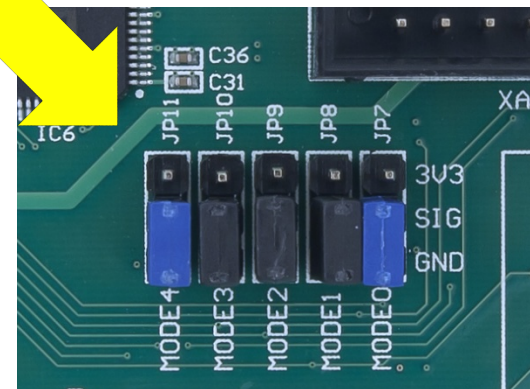
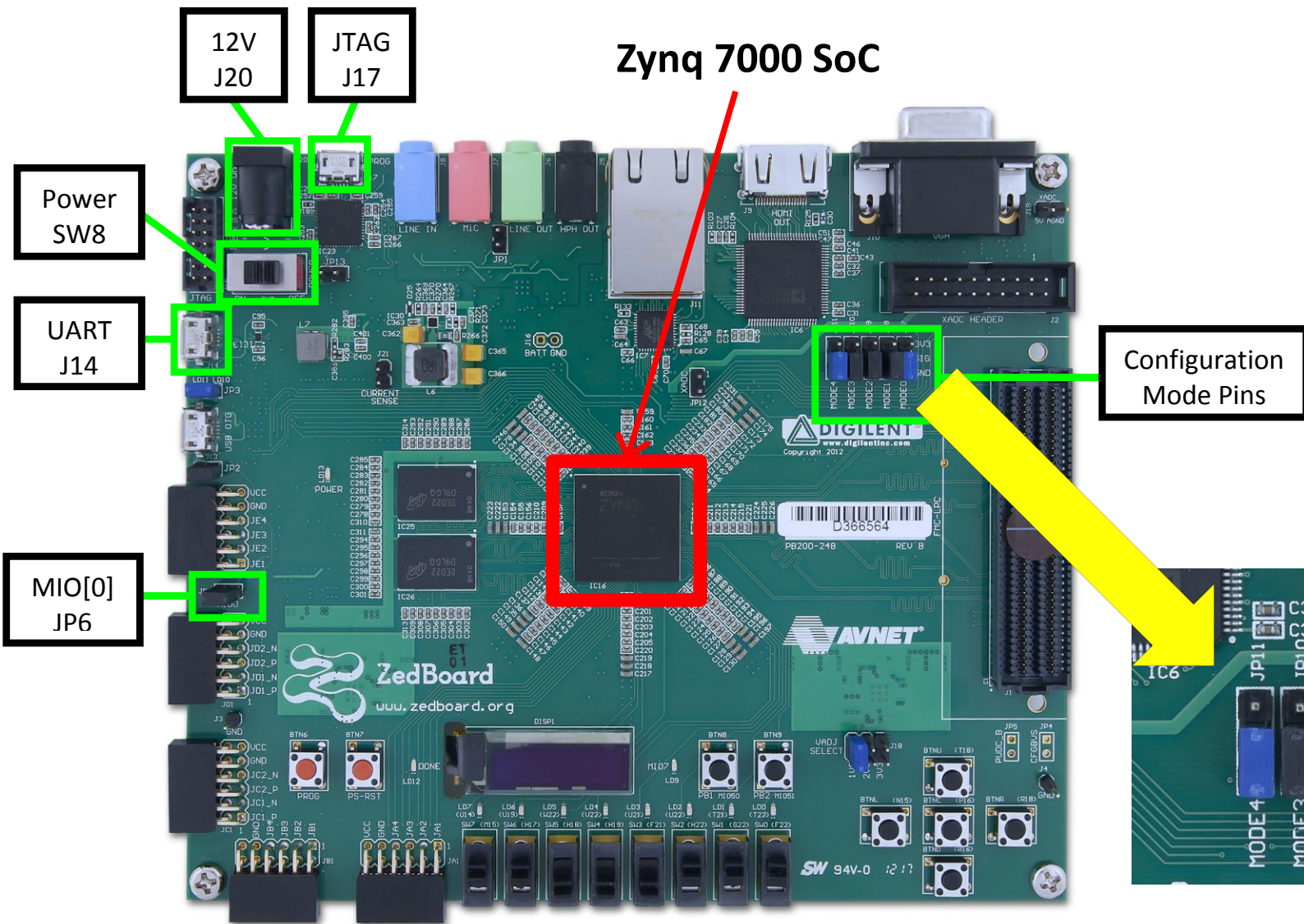


CDA 4253 FPGA System Design

Introduction to Zynq

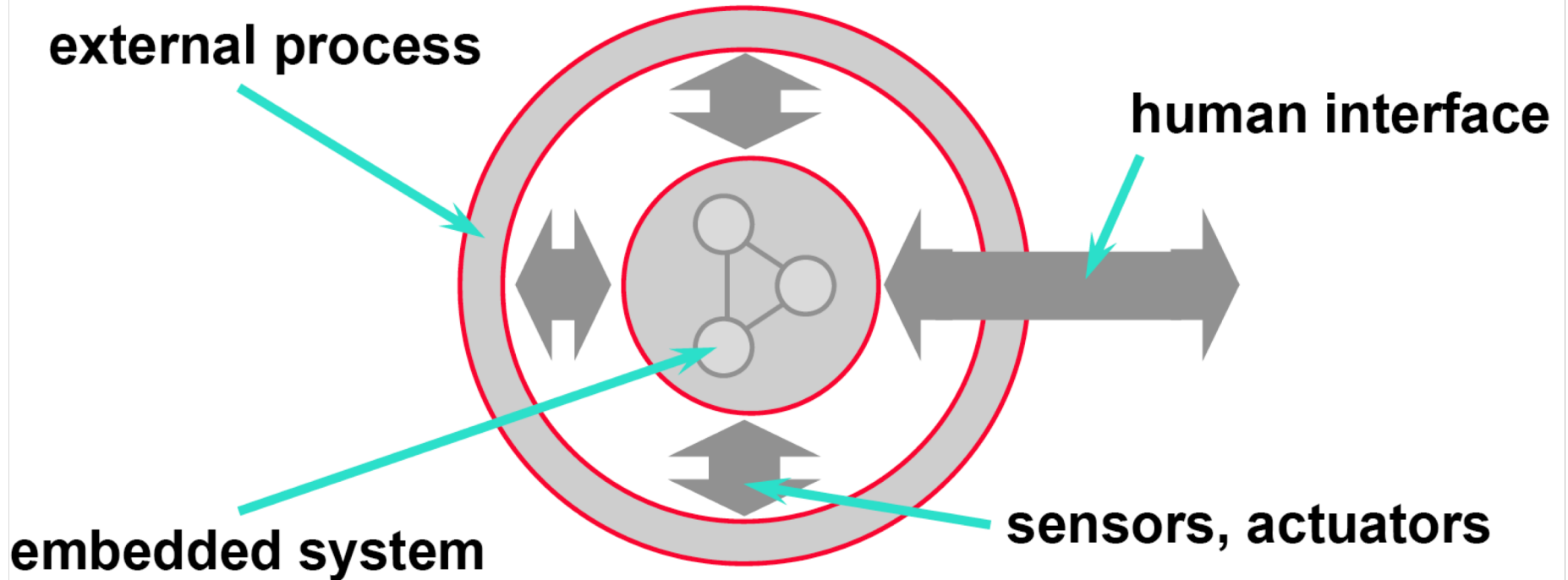
Hao Zheng
Dept of Comp Sci & Eng
U of South Florida



Key Features

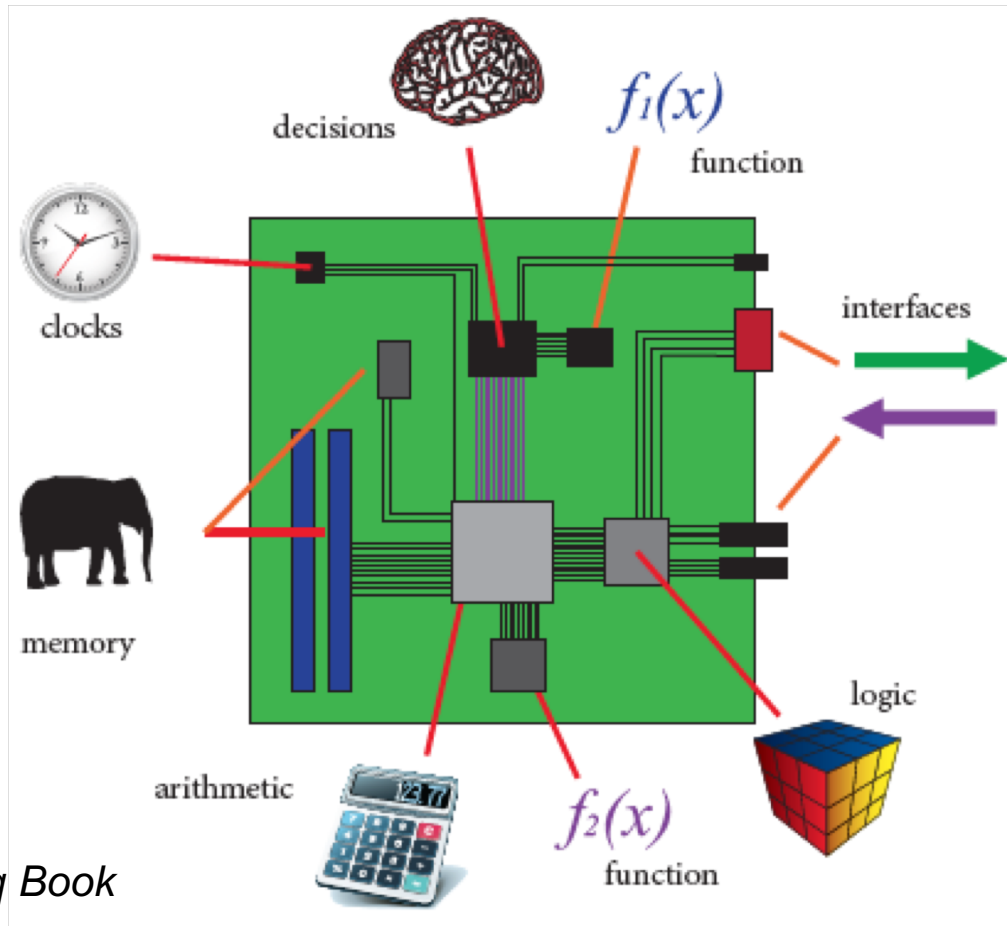
- Processor – Zynq-7000 AP SoC
- Memory
 - 512 MB DDR3
 - 256 Mb Quad-SPI Flash
 - 4GB SDcard
- Communication
 - Onboard USB-JTAG Programming
 - 10/100/1000 Ethernet
 - USB OTG 2.0 and USB-UART
- Expansion Ports – Pmods

A General View of Embedded Systems



Source: ETHZ, Prof. Lothar Thiele

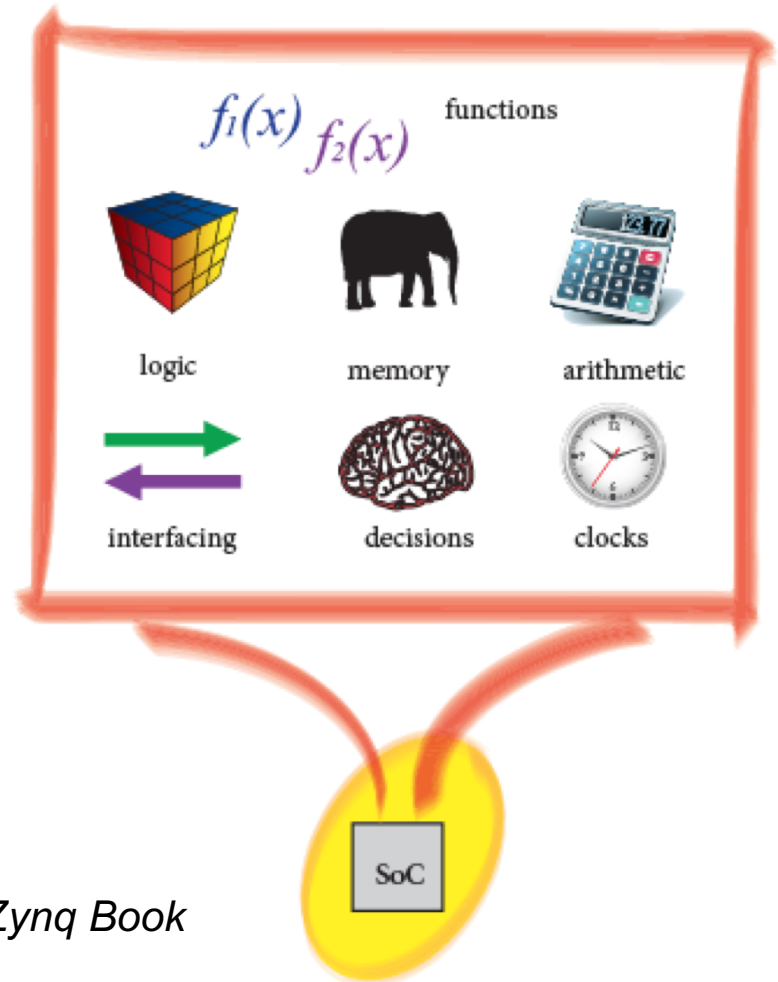
System-on-a-Board



Source: *The Zynq Book*

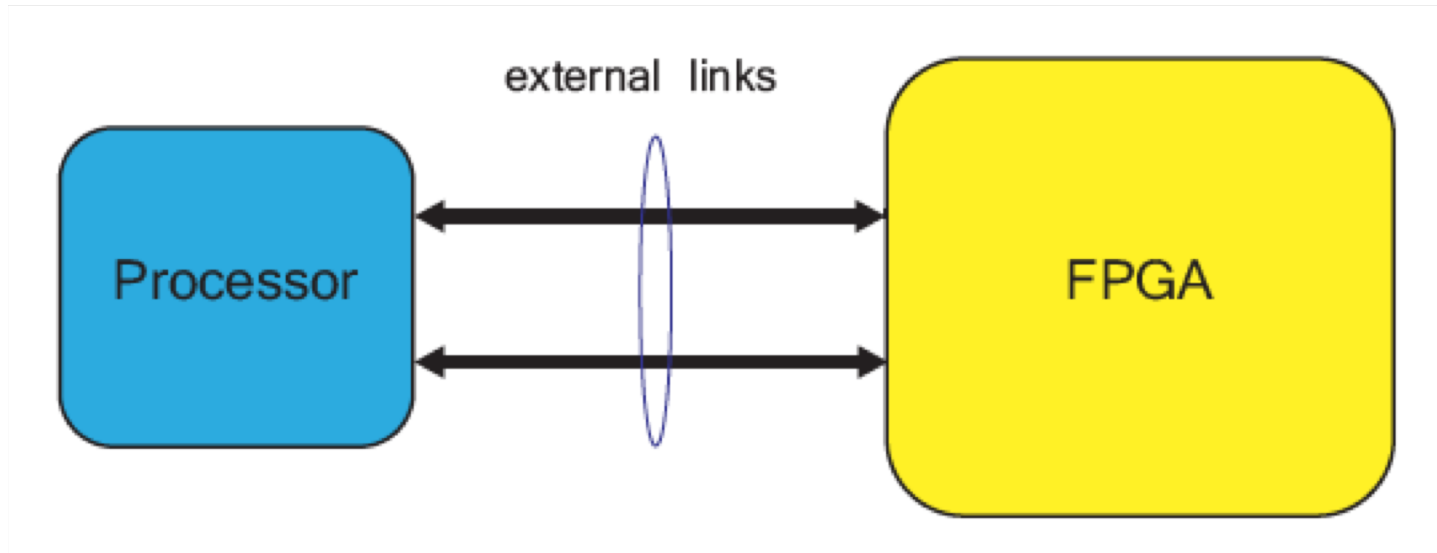
System-on-a-Chip (SoC)

- Higher performance
- Lower power use
- Small form factor
- Reduced cost
- flexibility



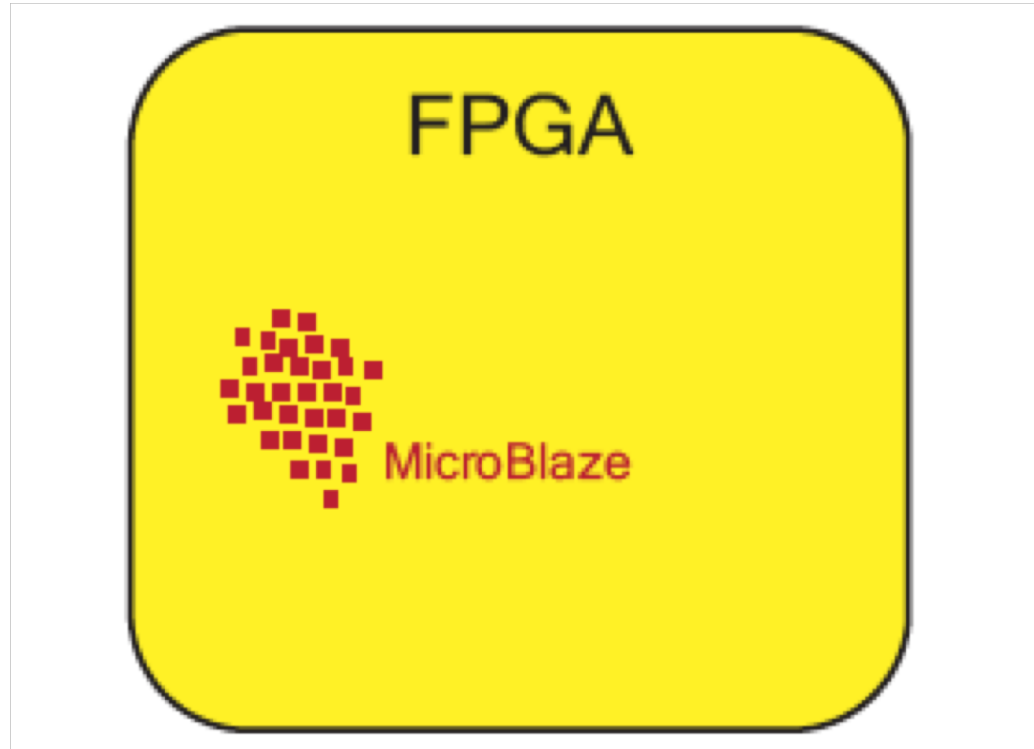
Source: *The Zynq Book*

How Are FPGAs used in the Past?



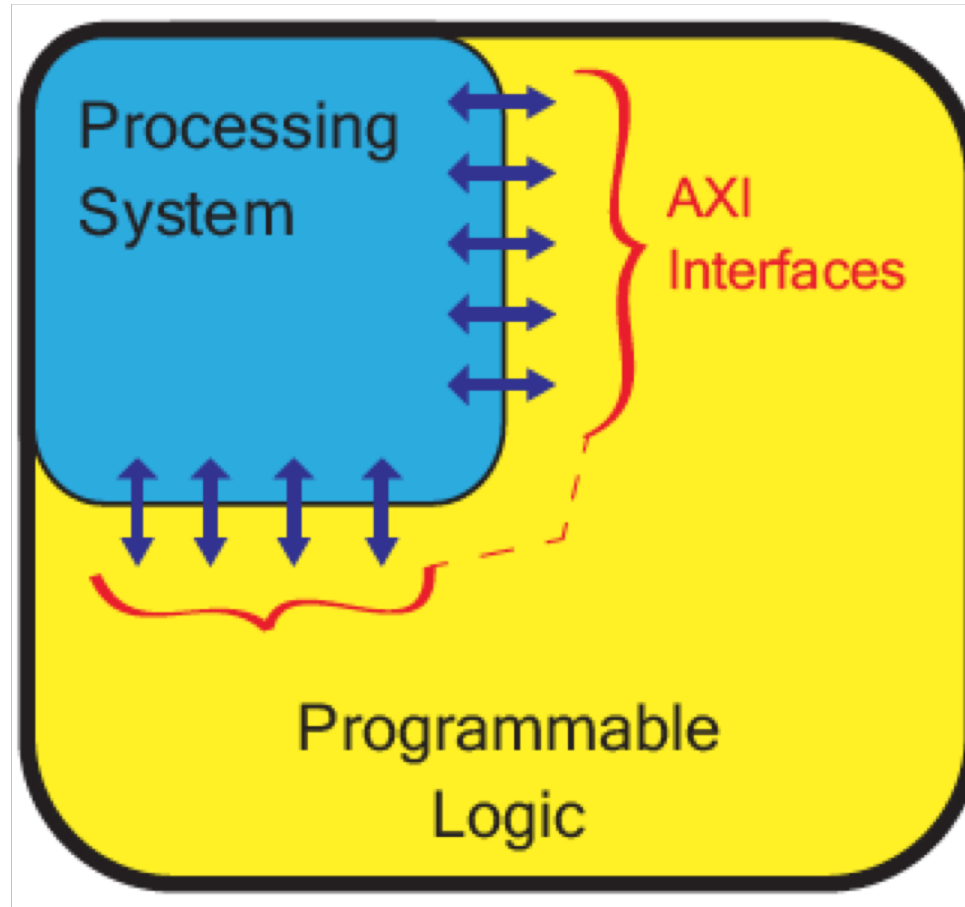
Source: *The Zynq Book*

How Are FPGAs used in the Past?



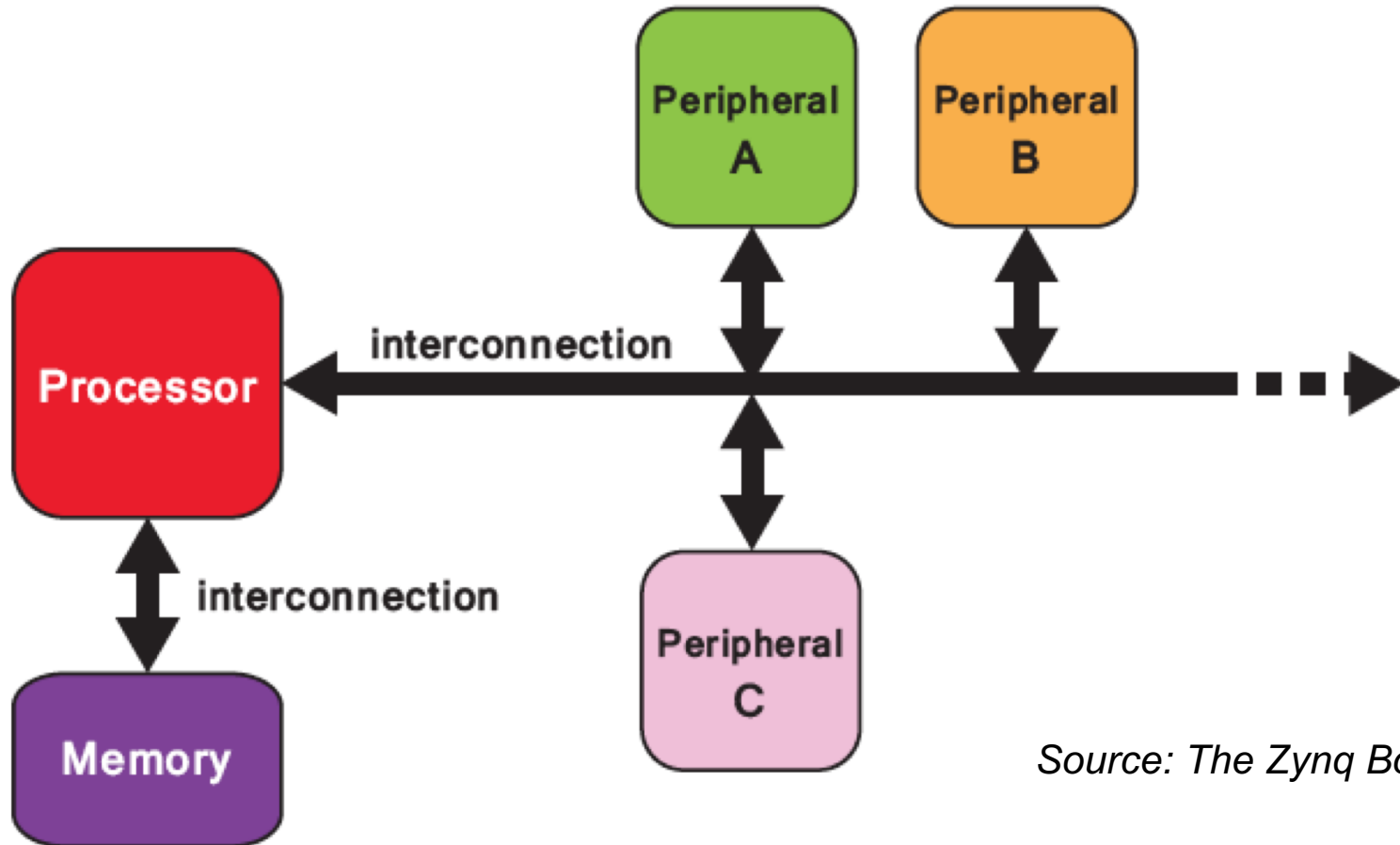
Source: The Zynq Book

Zynq – All Programmable SoC



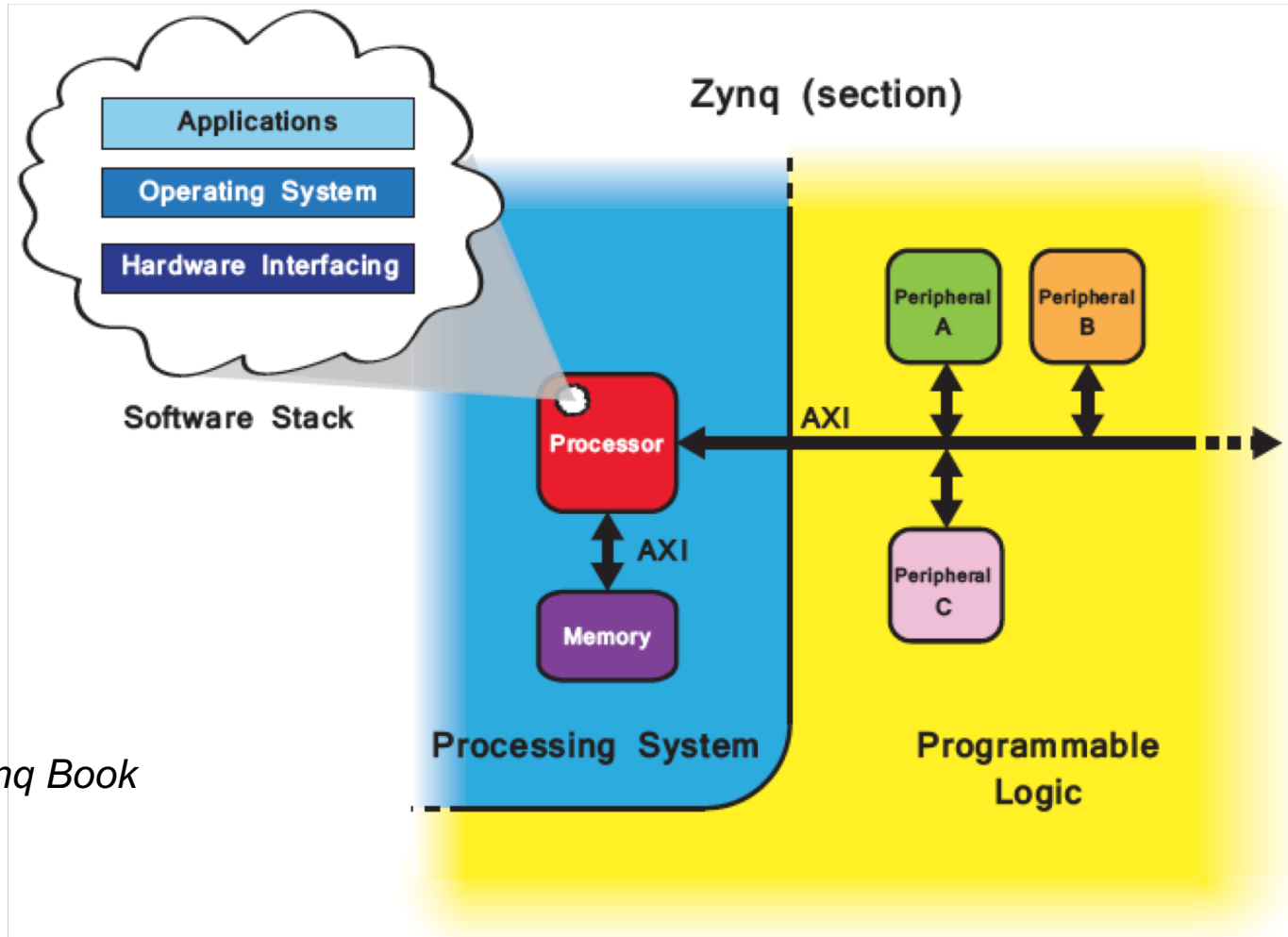
Source: *The Zynq Book*

Generic Embedded Architecture



Source: The Zynq Book

Generic Embedded Architecture – Mapping to Zynq



Source: *The Zynq Book*

Zynq 7000 SoC

- **Complete ARM®-based Processing System**

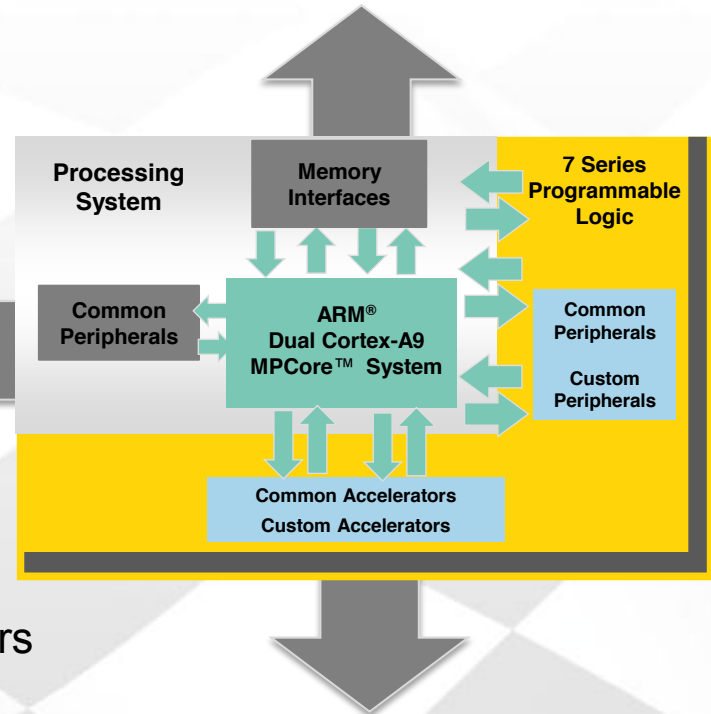
- Dual ARM Cortex™-A9 MPCore™, processor centric
- Integrated memory controllers & peripherals
- Fully autonomous to the Programmable Logic

- **Tightly Integrated Programmable Logic**

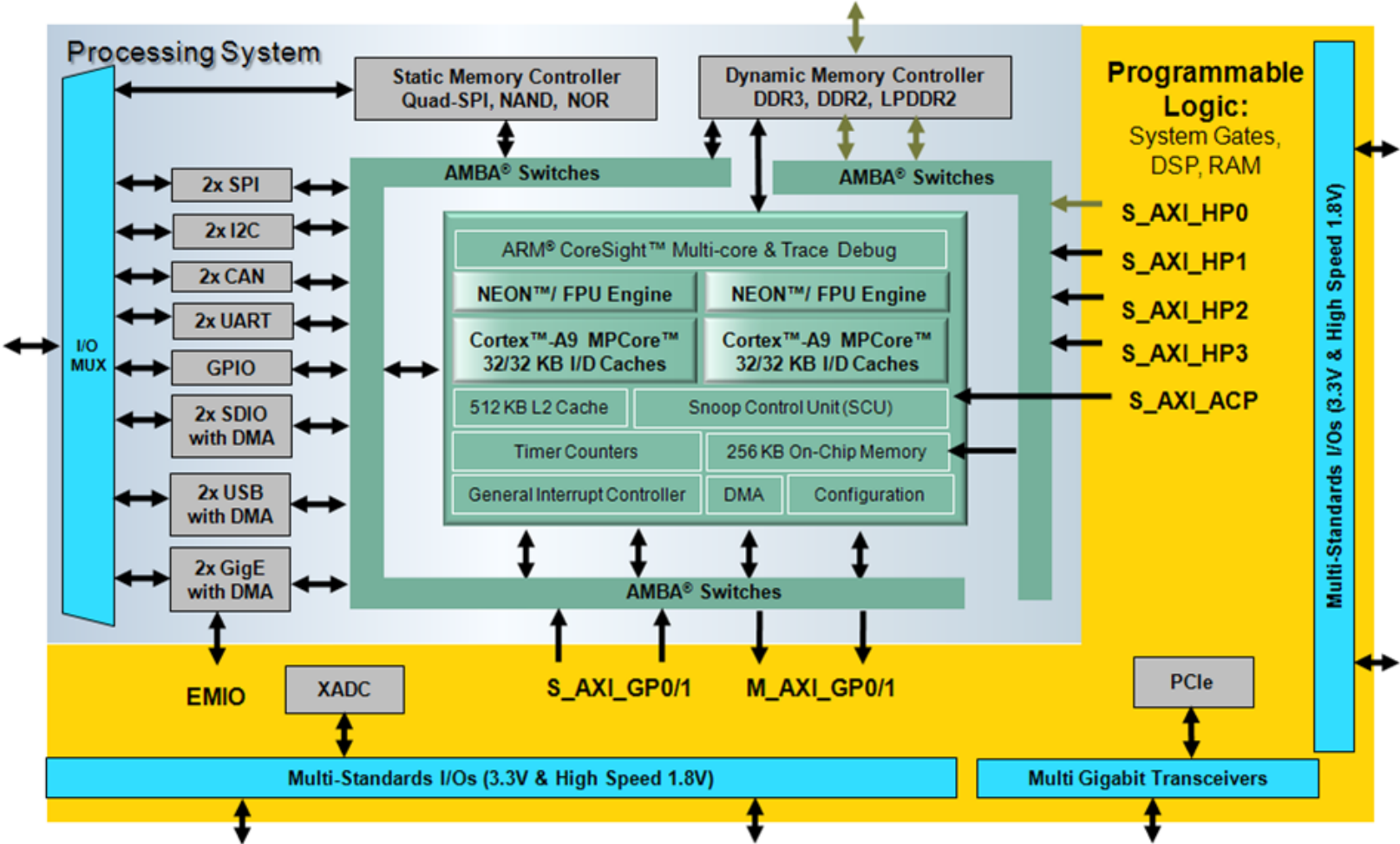
- Used to extend Processing System
- Scalable density and performance
- Over 3000 internal interconnects

- **Flexible Array of I/O**

- Wide range of external multi-standard I/O
- High performance integrated serial transceivers
- Analog-to-Digital Converter inputs



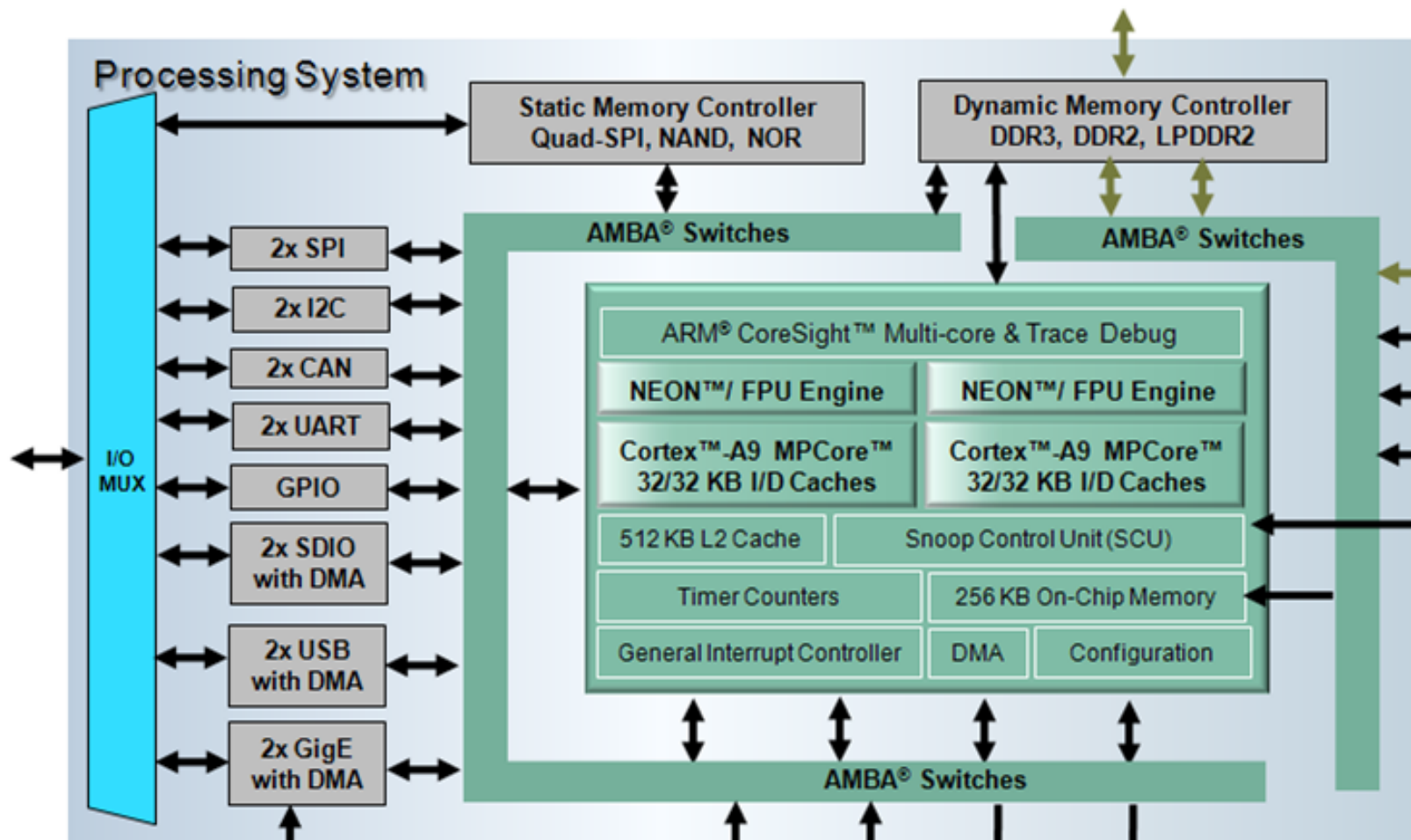
Zynq-7000 SoC Block Diagram



PS and PL

- PS: Processing system, hard silicon core
 - Dual ARM Cortex-A9 processor based
 - Multiple peripherals
- PL: Programmable logic
 - Shares the same 7 series programmable logic as
 - Artix-based devices: Z-7010 and **Z-7020** (high-range I/O banks only)
 - Kintex-based devices: Z-7030 and Z-7045 (mix of high-range and high-performance I/O banks)

PS Components

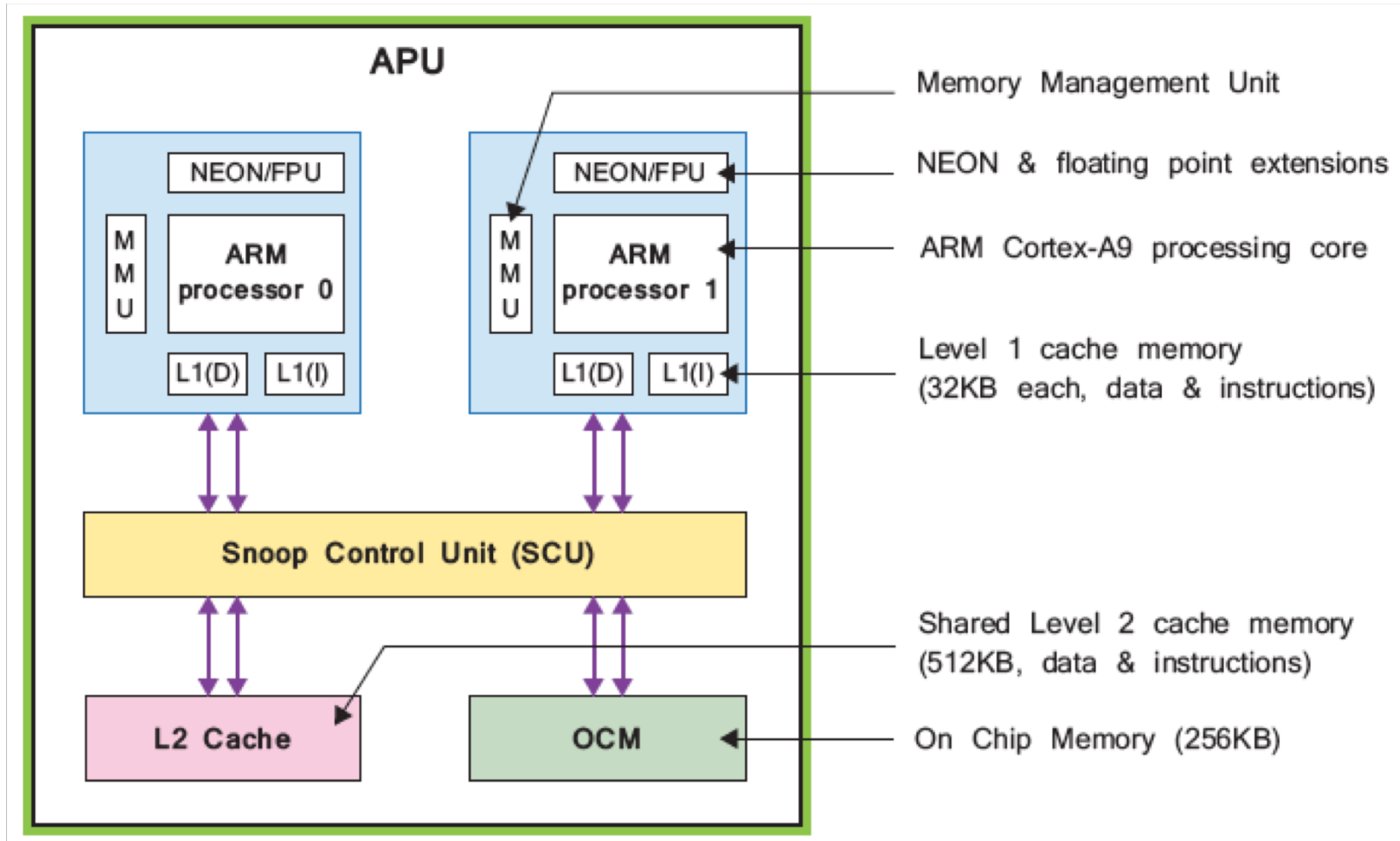


PS Components

- Application processing unit (APU)
- I/O peripherals
 - Multiplexed I/O (MIO),
 - extended multiplexed I/O (EMIO)
- Memory interfaces
- PS interconnect
- DMA
- Timers
- General interrupt controller (GIC)
- On-chip memory (OCM)
- Debug controller: ARM CoreSight

Block Diagram – APU

Source: *The Zynq Book*

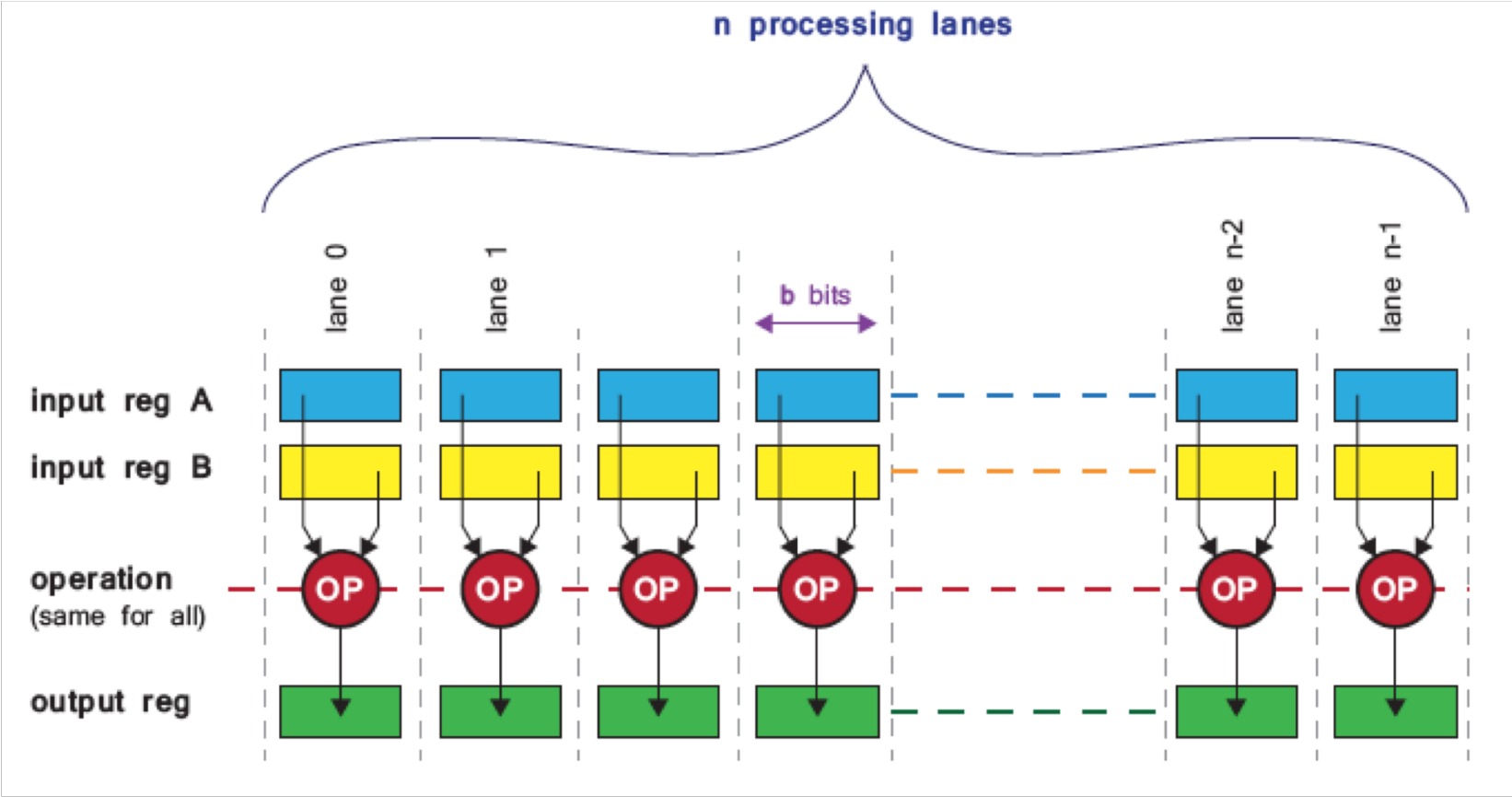


ARM Cortex–A9 Processor

- Dual-core processor cluster
- 2.5 DMIP/MHz per processor
- Harvard architecture
 - Self-contained 32KB L1 caches for instructions and data
- External memory based 512KB L2 cache
- Automatic cache coherency between processor cores
- Up to 1 GHz operation (fastest speed grade)

Architecture – NEON

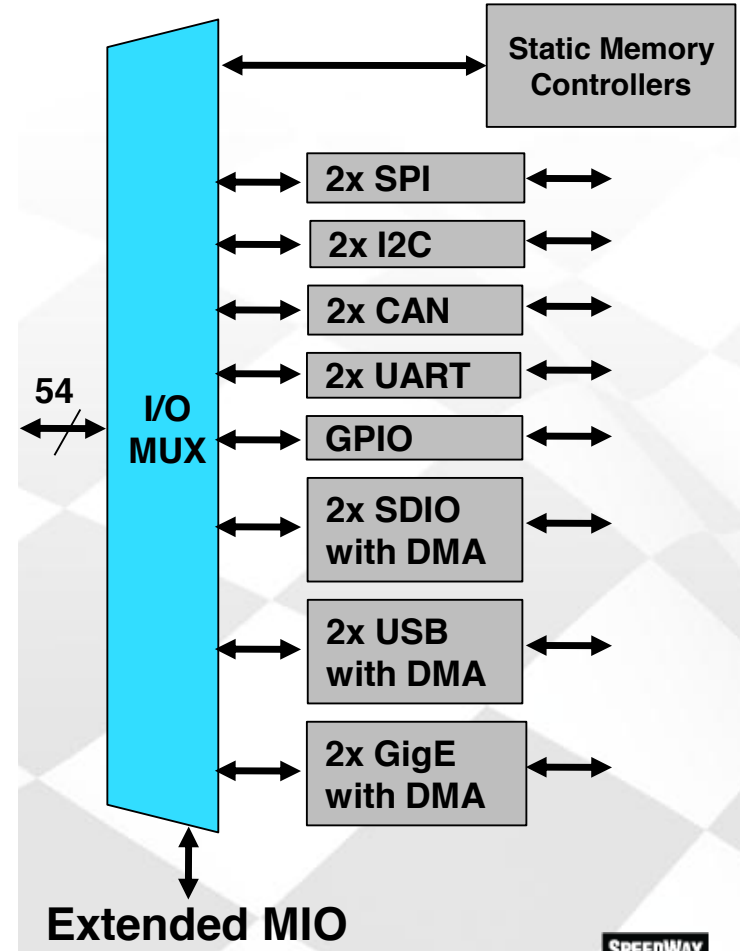
Source: *The Zynq Book*



For image and video processing

PS Peripherals

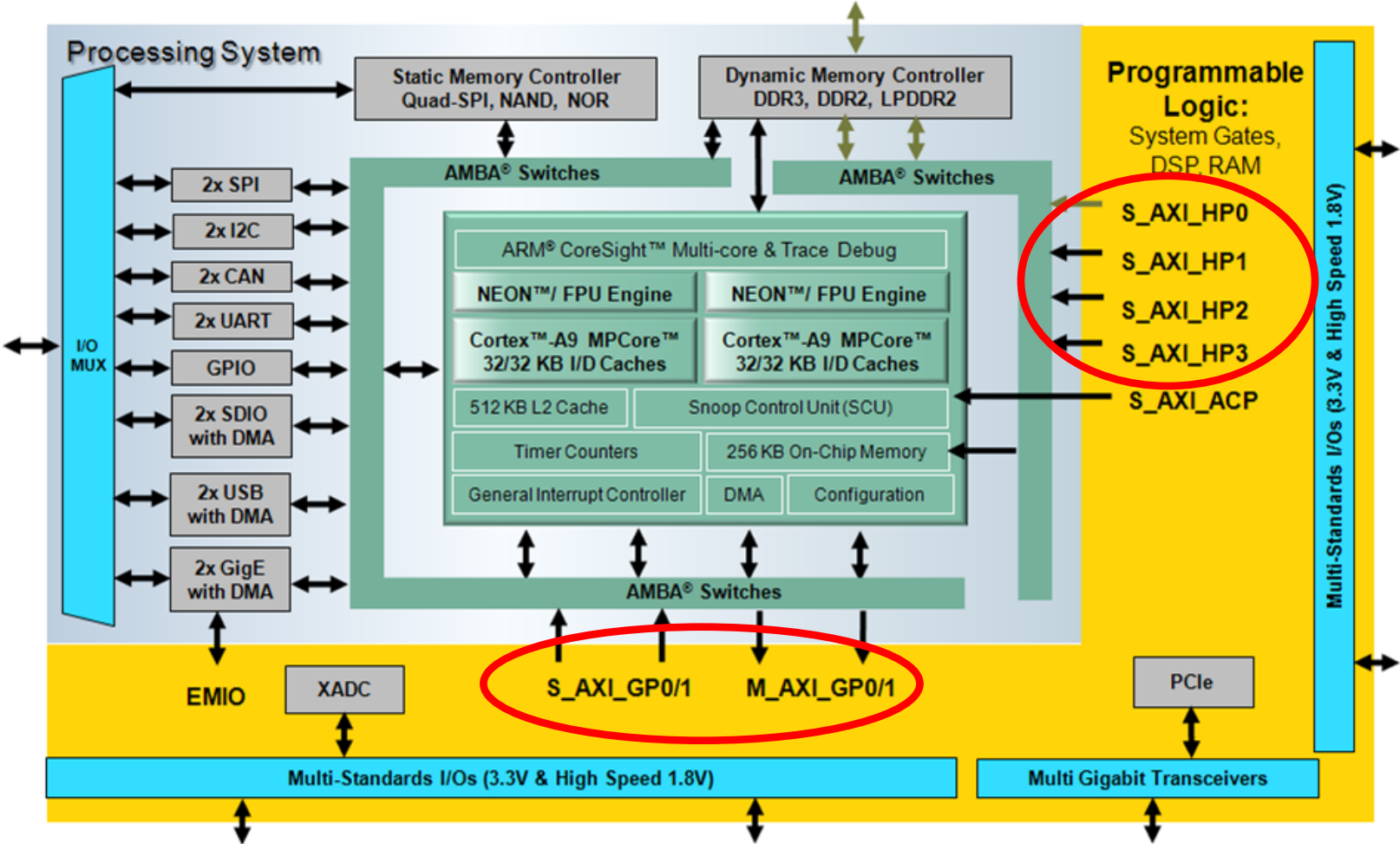
- Multiplexed Input/Output (MIO)
 - Multiplexed output of peripheral and static memories
- Extended MIO
 - Extension with PL side IOs
 - Additional interface with PL cores



PS – PL Interface

- **AXI high-performance slave ports (HP0-HP3)**
 - Configurable 32-bit or 64-bit data width
 - Access to OCM and DDR only
 - Conversion to processing system clock domain
 - AXI FIFO Interface (AFI) are FIFOs (1KB) to smooth large data transfers
- **AXI general-purpose ports (GP0-GP1)**
 - Two masters from PS to PL
 - Two slaves from PL to PS
 - 32-bit data width
 - Conversation and sync to processing system clock domain

Zynq-7000 SoC Block Diagram



PS – PL Interface

Interface Name	Interface Description	Master	Slave
M_AXI_GP0	General Purpose (AXI_GP)	PS	PL
M_AXI_GP1		PS	PL
S_AXI_GP0	General Purpose (AXI_GP)	PL	PS
S_AXI_GP1		PL	PS
S_AXI_ACP	Accelerator Coherency Port (ACP), cache coherent transaction	PL	PS
S_AXI_HP0	High Performance Ports (AXI_HP) with read/write FIFOs. (Note that AXI_HP interfaces are sometimes referred to as AXI Fifo Interfaces, or AFIs).	PL	PS
S_AXI_HP1		PL	PS
S_AXI_HP2		PL	PS
S_AXI_HP3		PL	PS

PS – PL Interface

- DMA, interrupts, events signals
 - Processor event bus for signaling event information to the CPU
 - PL peripheral IP interrupts to the PS general interrupt controller (GIC)
- Extended multiplexed I/O (EMIO) allows PS peripheral ports access to PL logic and device I/O pins

Memory Map

- The Cortex-A9 processor uses 32-bit addressing
- All PS/PL peripherals are memory mapped to the A9 cores
- All PL slave peripherals are located between
 - 4000_0000 -- 7FFF_FFFF (connected to GP0)
 - 8000_0000 -- BFFF_FFFF (connected to GP1)

FFFC_0000 to FFFF_FFFF

FD00_0000 to FFFB_FFFF

FC00_0000 to FCFF_FFFF

F8F0_3000 to FBFF_FFFF

F890_0000 to F8F0_2FFF

F801_0000 to F88F_FFFF

F800_1000 to F880_FFFF

F800_0C00 to F800_0FFF

F800_0000 to F800_0BFF

E600_0000 to F7FF_FFFF

E100_0000 to E5FF_FFFF

E030_0000 to E0FF_FFFF

E000_0000 to E02F_FFFF

C000_0000 to DFFF_FFFF

8000_0000 to BFFF_FFFF

4000_0000 to 7FFF_FFFF

0010_0000 to 3FFF_FFFF

0004_0000 to 000F_FFFF

0000_0000 to 0003_FFFF

OCM

Reserved

Quad SPI linear address

Reserved

CPU Private registers

Reserved

PS System registers,

Reserved

SLCR Registers

Reserved

SMC Memory

Reserved

IO Peripherals

Reserved

PL (MAXI_GP1)

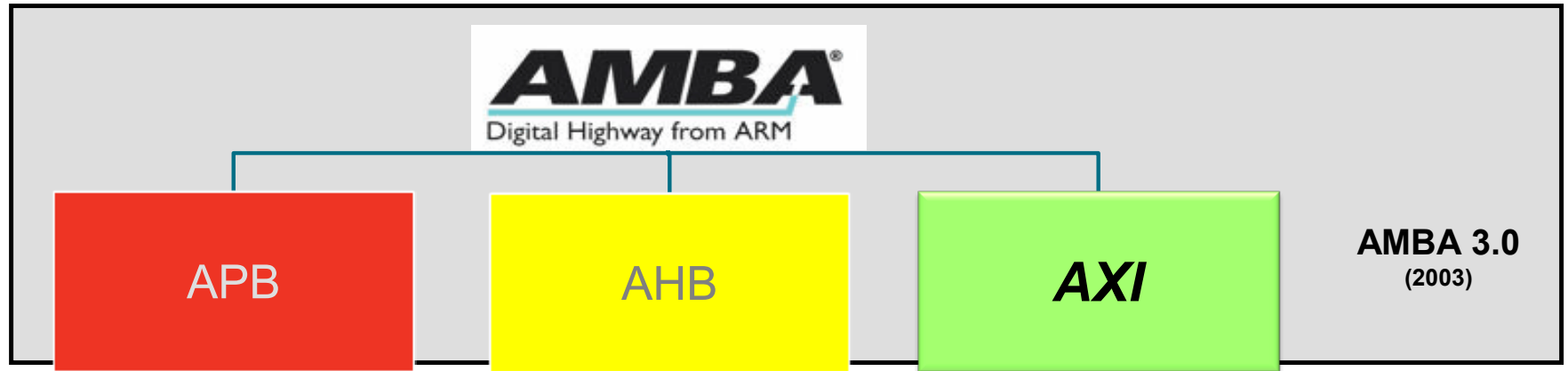
PL (MAXI_GP0)

DDR(address not filtered by SCU)

DDR(address filtered by SCU)

OCM

AXI Interface



AMBA: Advanced Microcontroller Bus Architecture

AXI: Advanced Extensible Interface

Basic AXI Protocol

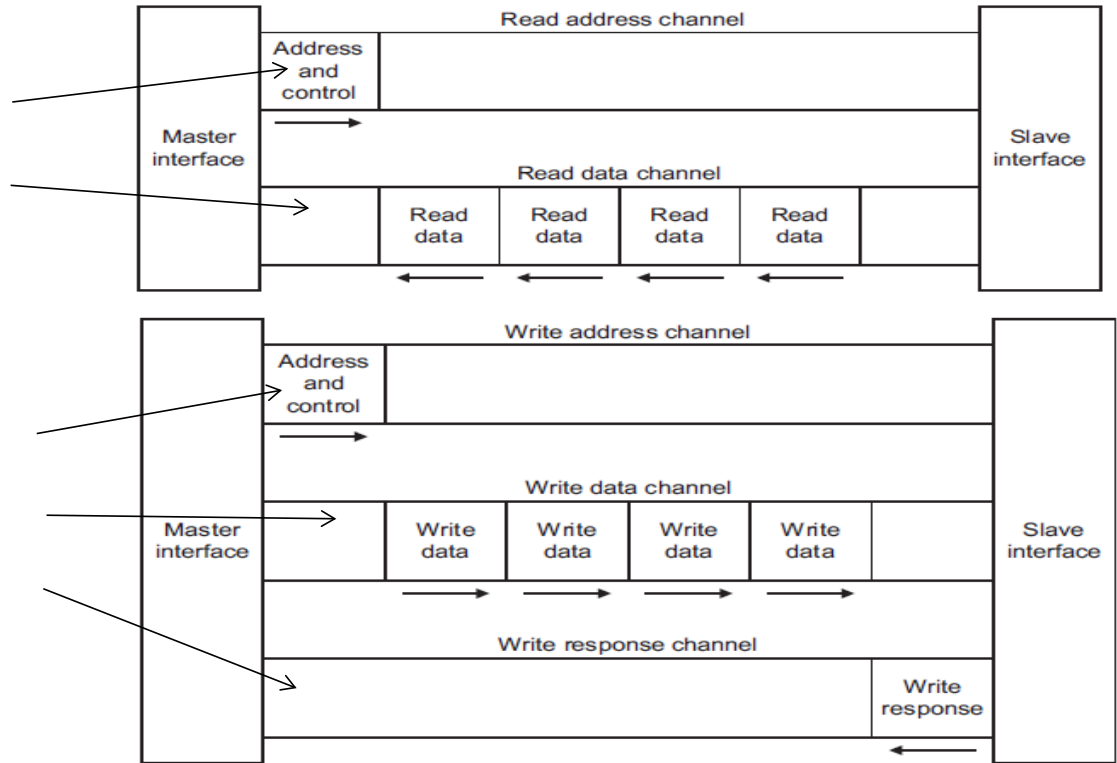
1. Read Address Channel

2. Read Data Channel

3. Write Address Channel

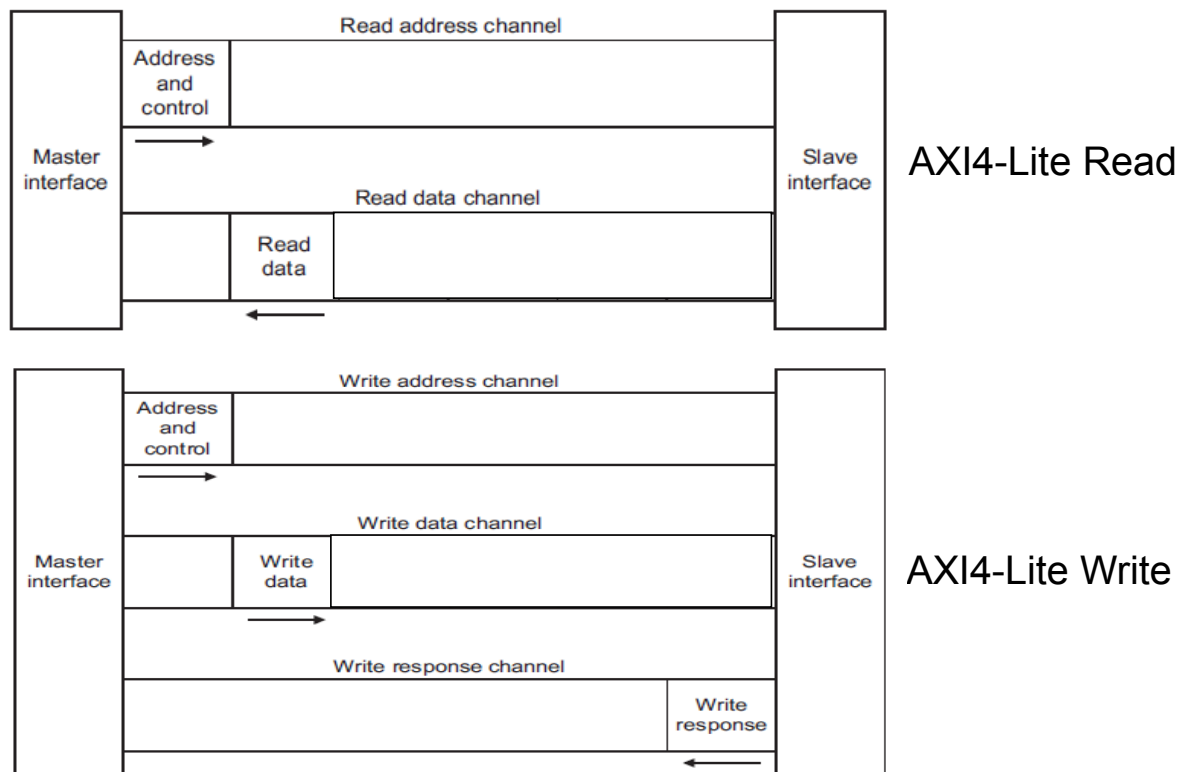
4. Write Data Channel

5. Write Response Channel



AXI4—Lite Protocol

- No burst
- Data width 32 or 64 only
 - Xilinx IP only supports 32-bits
- Very small footprint
- Bridging to AXI4 handled automatically by AXI_Interconnect (if needed)



AXI4 Protocol

➤ Sometimes called “Full AXI” or Memory Mapped”

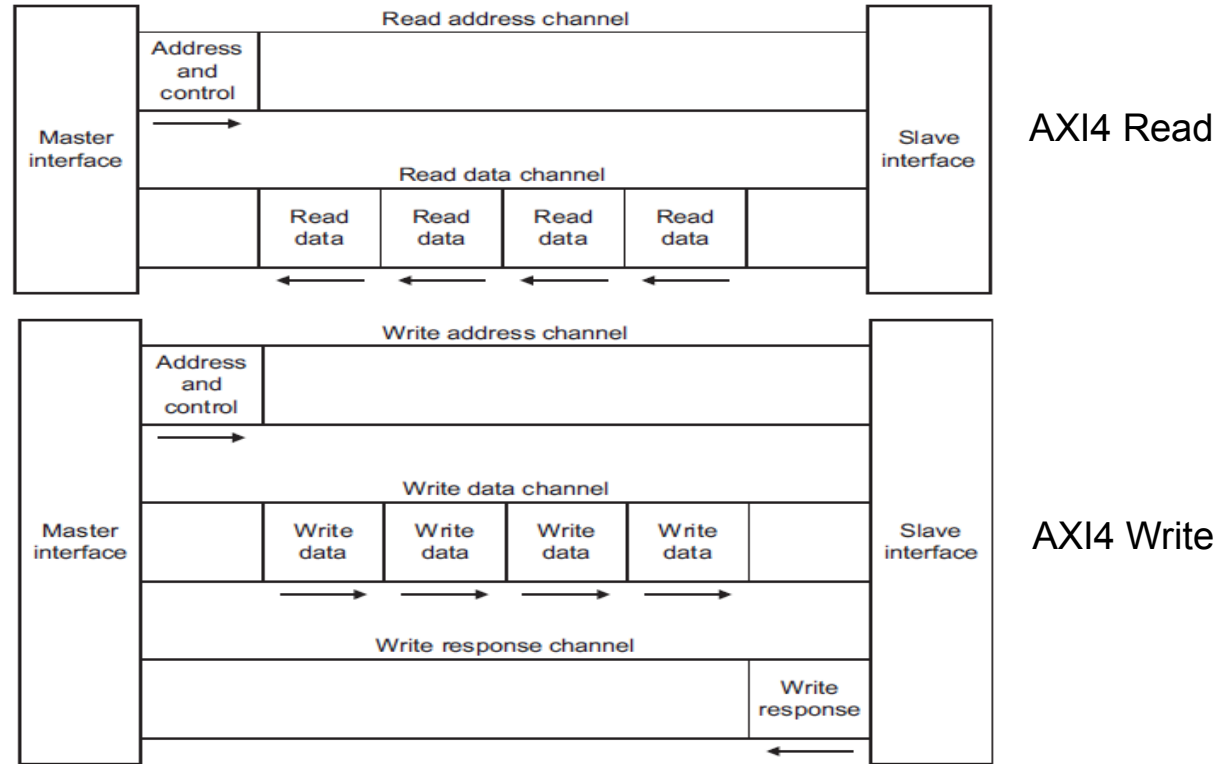
- Not ARM-sanctioned names

➤ Single address multiple data

- Burst up to 256 data beats

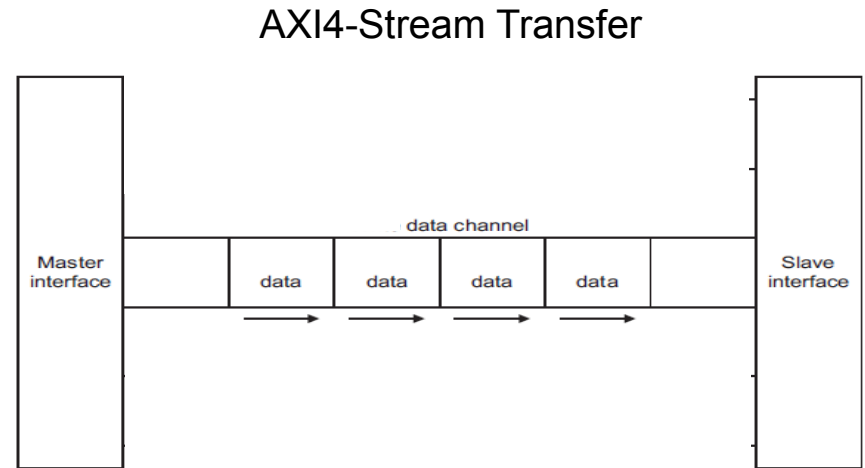
➤ Data Width parameterizable

- 1024 bits

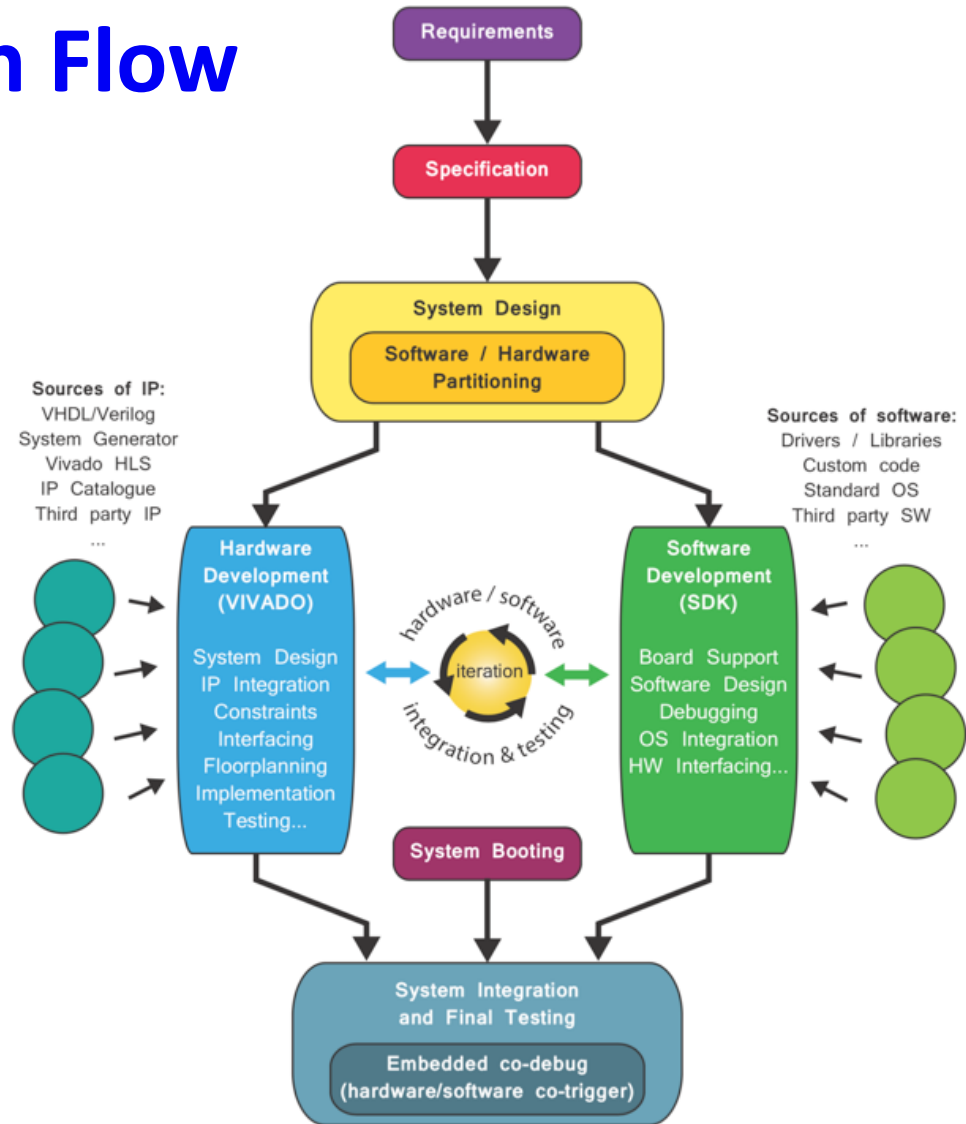


AXI4—Stream Protocol

- **No address channel, no read and write, always just master to slave**
 - Effectively an AXI4 “write data” channel
- **Unlimited burst length**
 - AXI4 max 256
 - AXI4-Lite does not burst
- **Virtually same signaling as AXI Data Channels**
 - Protocol allows merging, packing, width conversion
 - Supports sparse, continuous, aligned, unaligned streams

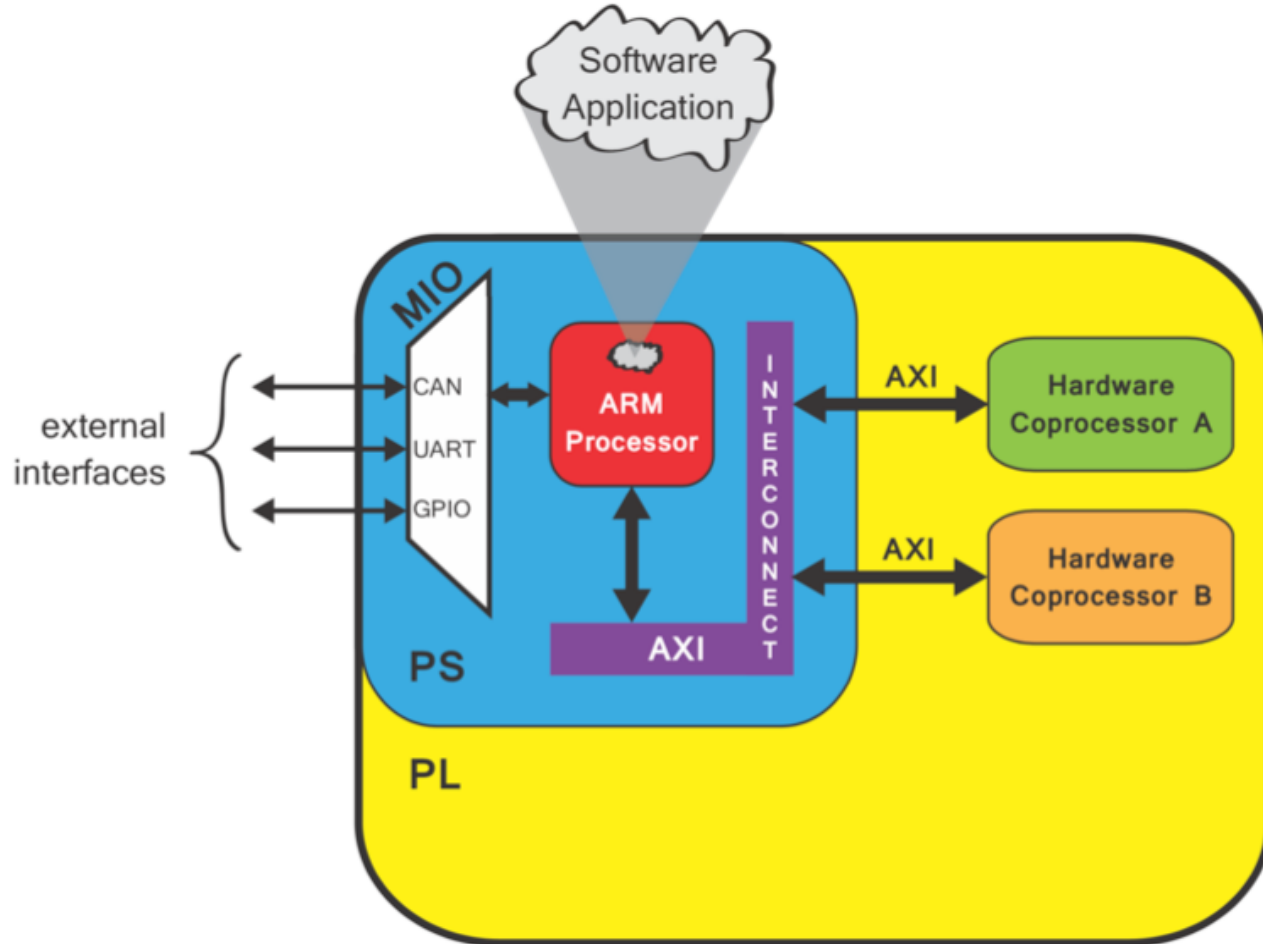


Basic Zynq Design Flow

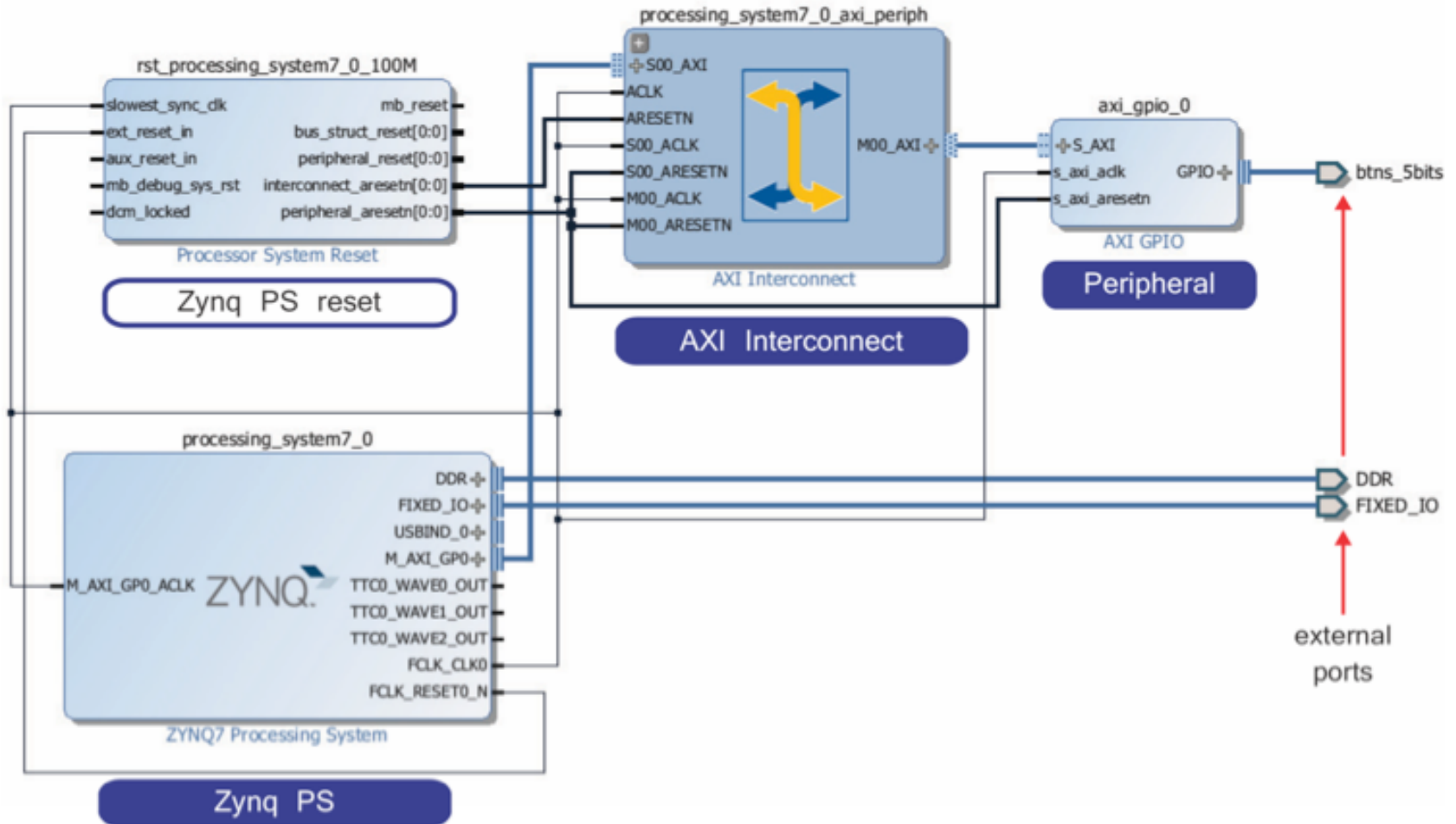


Source: The Zynq Book

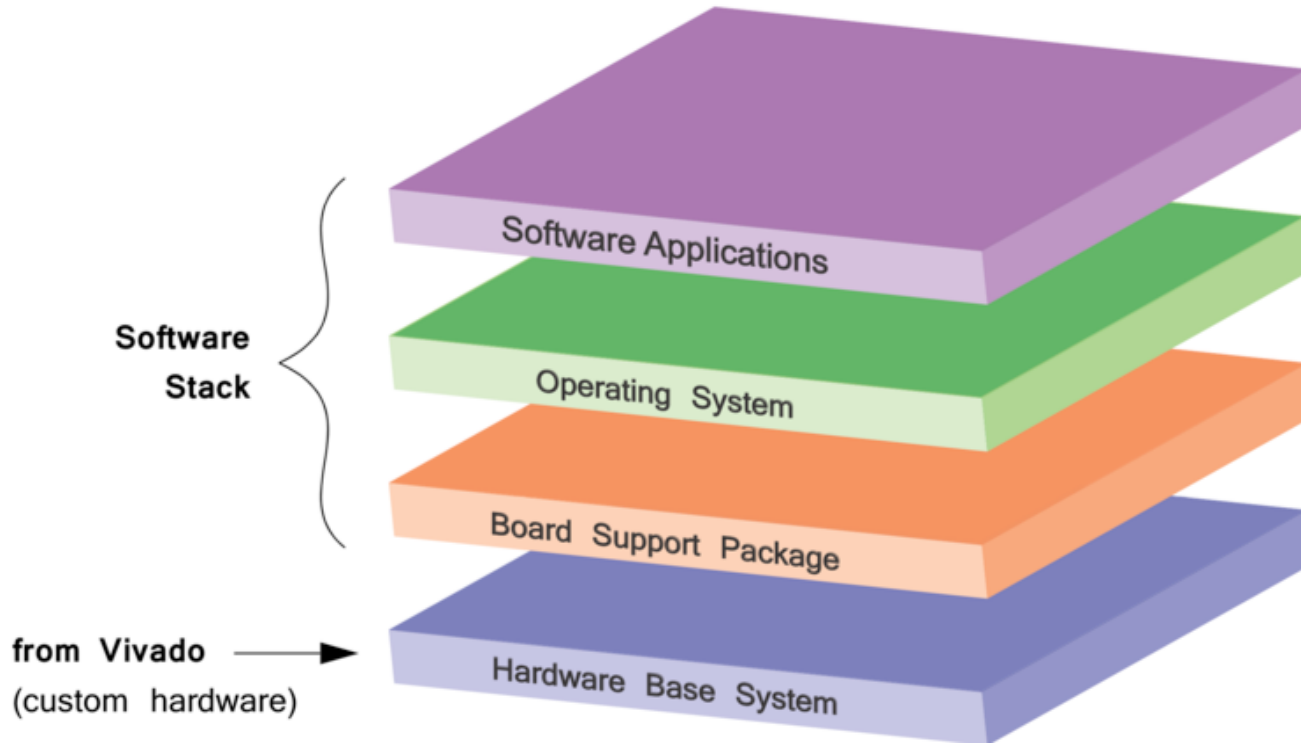
Hardware Development



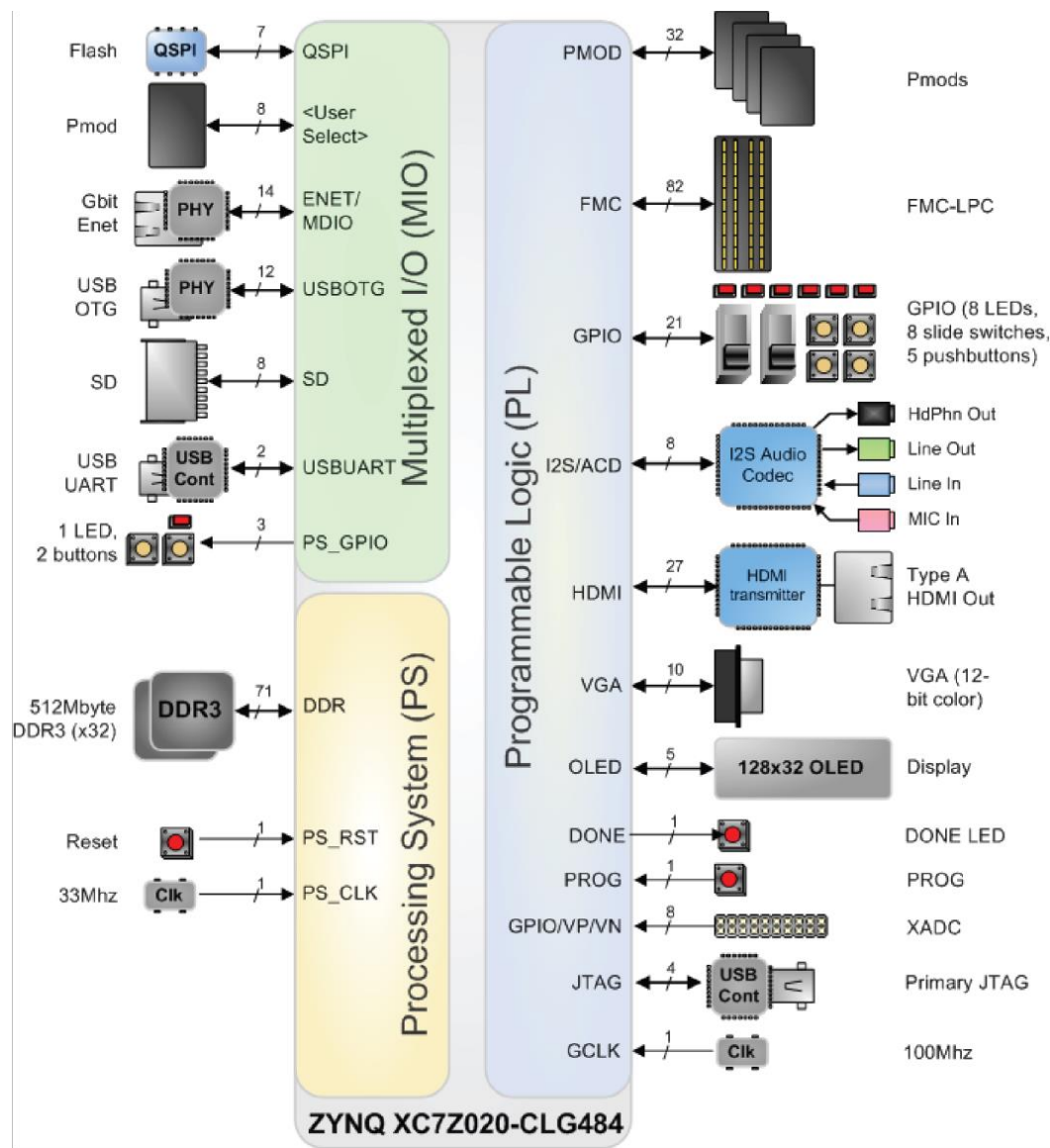
Hardware Development



Software Development



- BSP includes low-level SW routing interfacing with HW
- Refreshed by SDK when HW base is changed



References

- [Zedboard Hardware User Guide](#)
- [The Zynq Book](#)
 - Chapter 1, 2, 3
- [The Zynq 7000 SoC Technical Reference Manual](#)