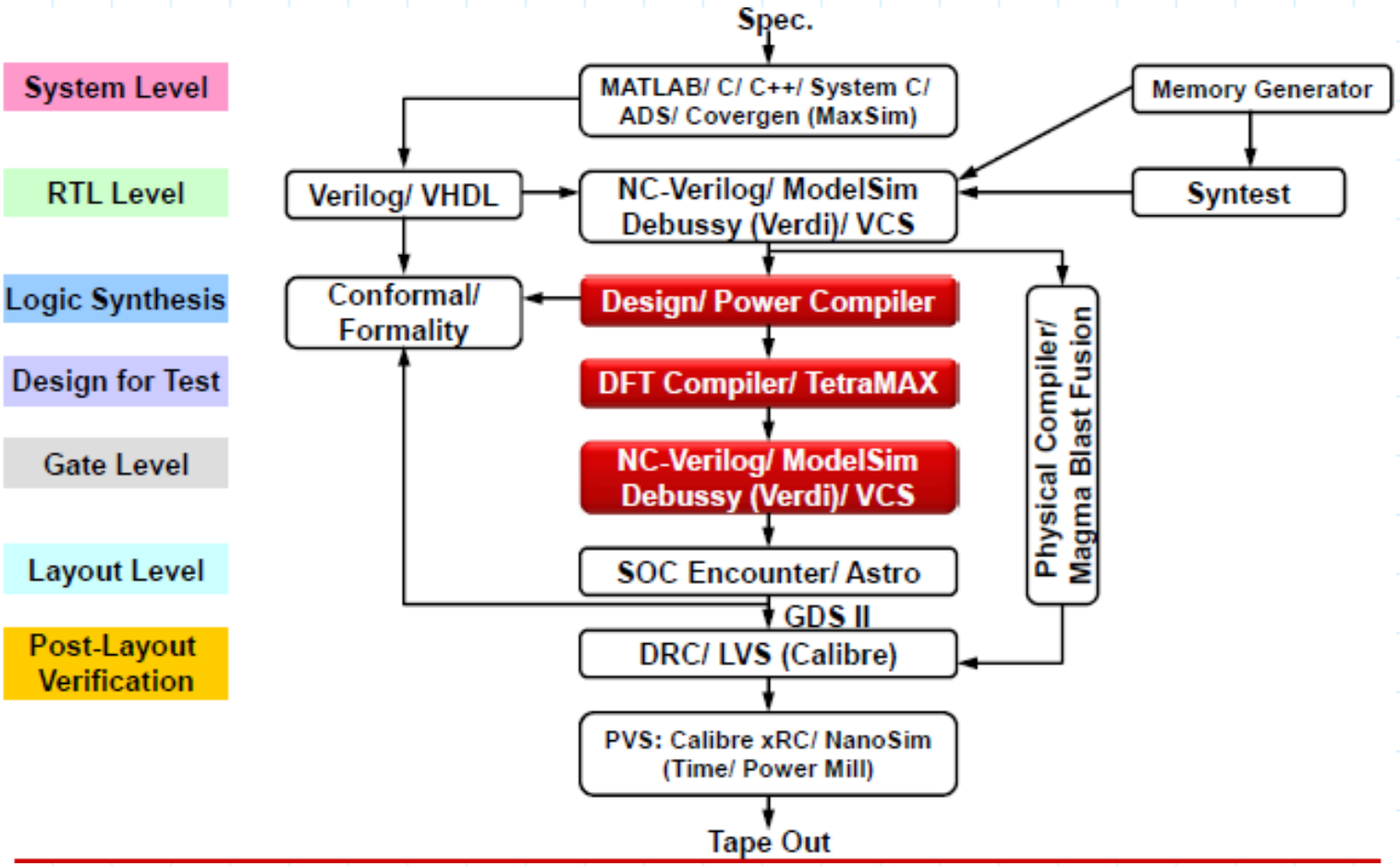
Βασικές αρχές της Synthesis

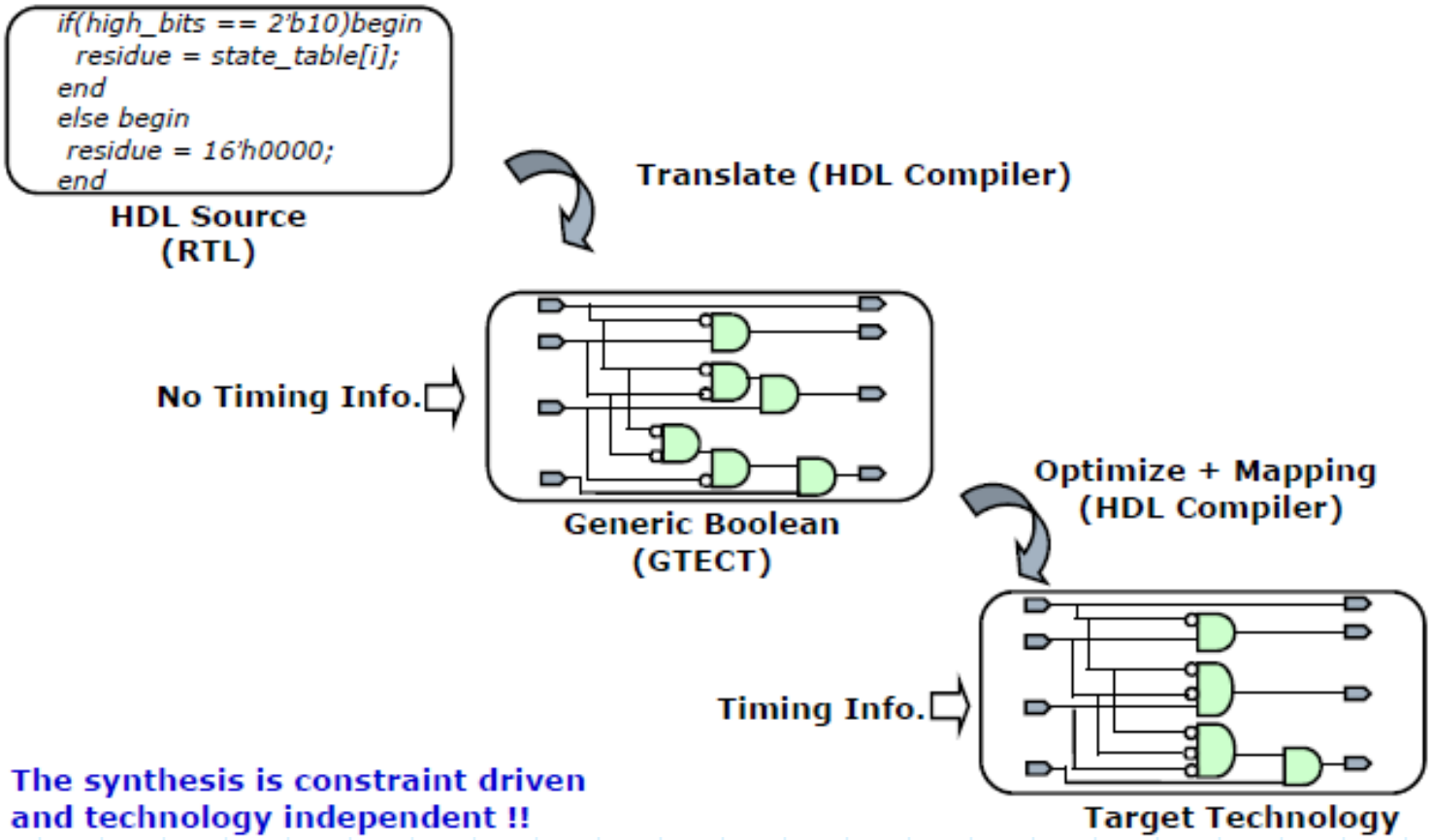
G.Kornaros

Cell based design flow

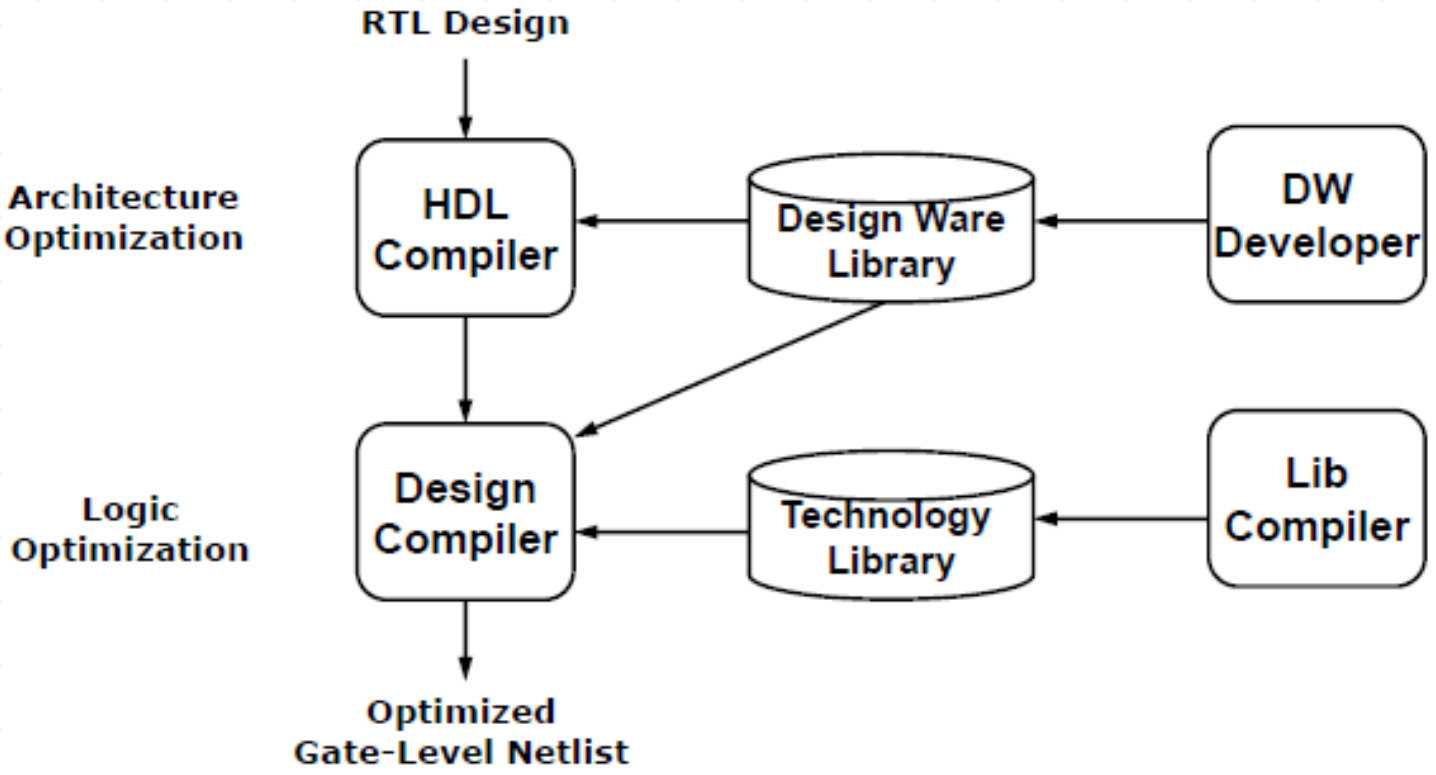


Τι είναι synthesis

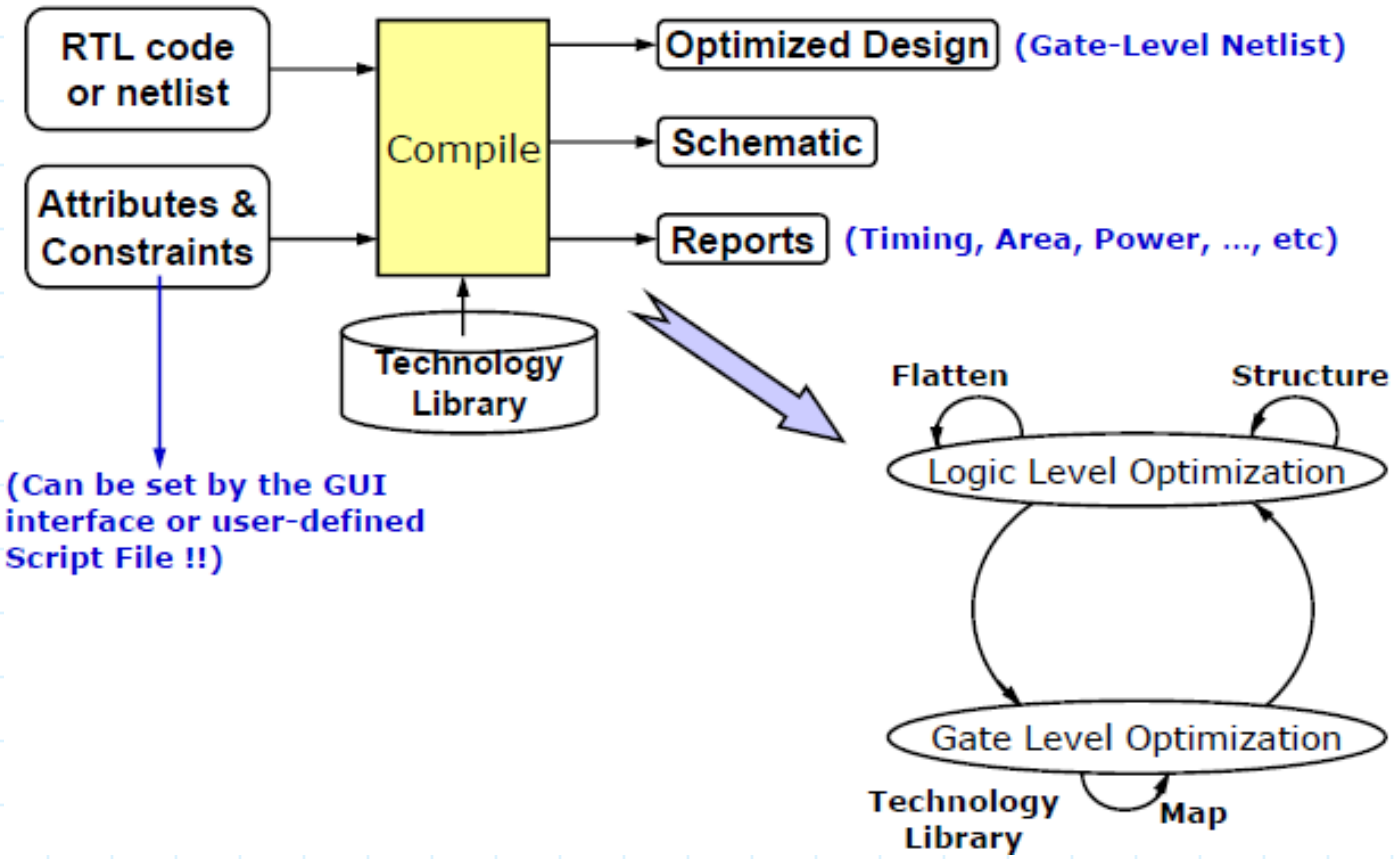
- Synthesis = translation + optimization + mapping



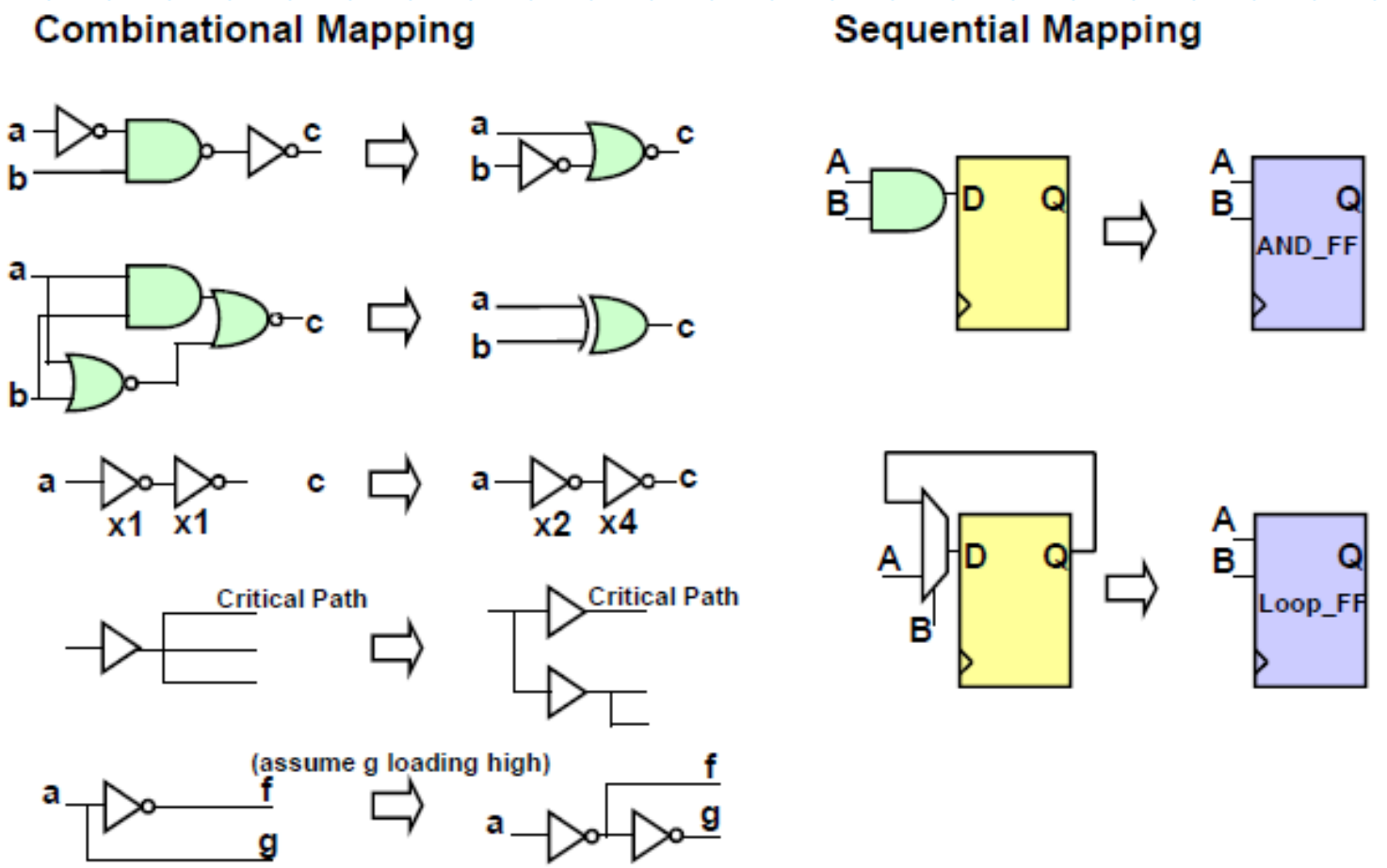
Logic synthesis



Synthesis ≈ *Compile*



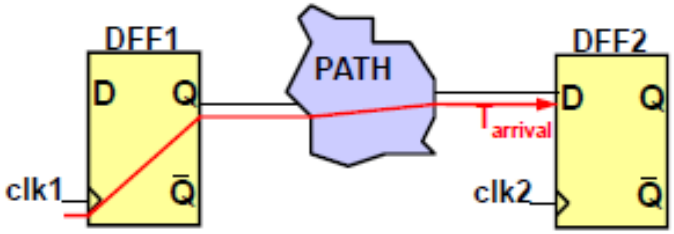
Optimizations - Mapping

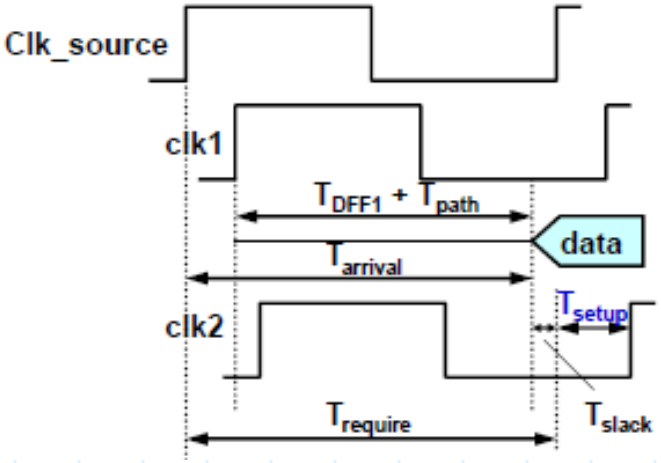


Static timing analysis (setup time)

- To meet the setup time requirement:
  - $T_{require} >= T_{arrival}$
- Reg to Reg
  - $T_{arrival} = T_{clk1} + T_{DFF1(clk->Q)} + T_{PATH}$
  - $T_{require} = T_{clk2} - T_{DFF2(setup)}$
  - $T_{slack} = T_{require} - T_{arrival}$

(T_{slack} > 0 denotes "no timing violation")





Static timing analysis (setup time)

- PI to Reg
  - $T_{arrival} = T_{PI(delay)} + T_{PATH}$
  - $T_{require} = T_{clk1} - T_{DFF1(setup)}$
  - $T_{slack} = T_{require} - T_{arrival}$