ΕΛΜΕΠΑ ΤΜΗΜΑ ΗΛΕΚΤΡΟΝΙΚΩΝ ΜΗΧΑΝΙΚΩΝ ΧΑΝΙΑ

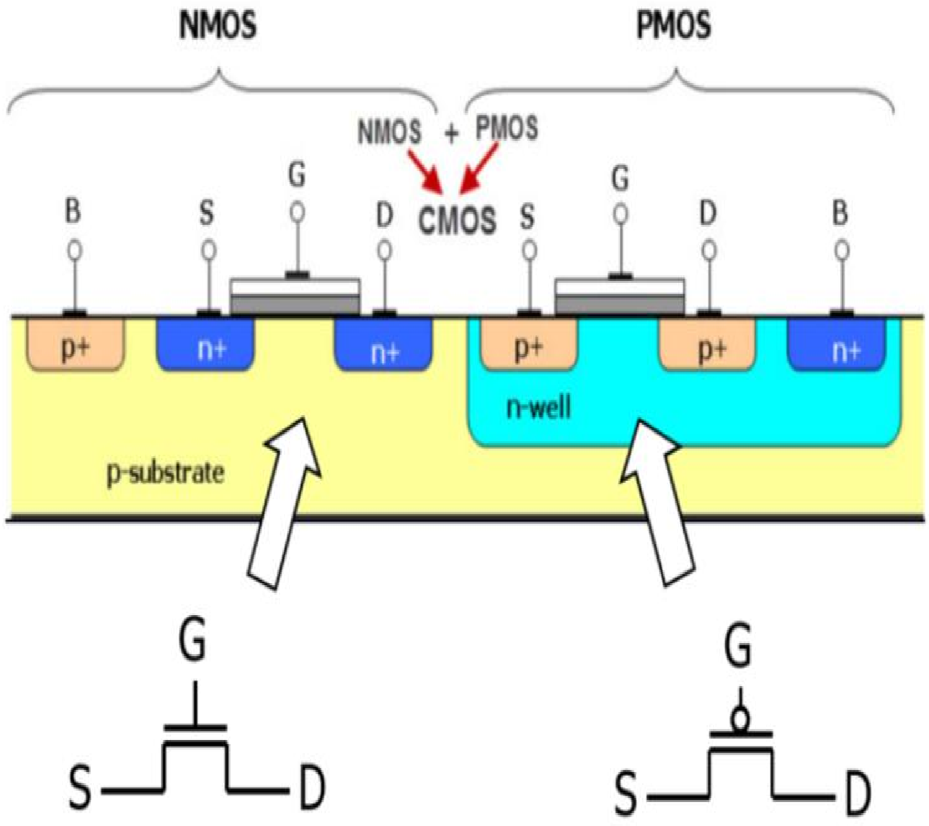
ΣΥΜΠΛΗΡΩΜΑΤΙΚΕΣ ΣΗΜΕΙΩΣΕΙΣ ΕΡΓΑΣΤΗΡΙΟΥ ΜΙΚΡΟΗΛΕΚΤΡΟΝΙΚΗΣ & VLSI

ΜΕΡΟΣ Β

ΣΤΟΙΧΕΙΟ MOS

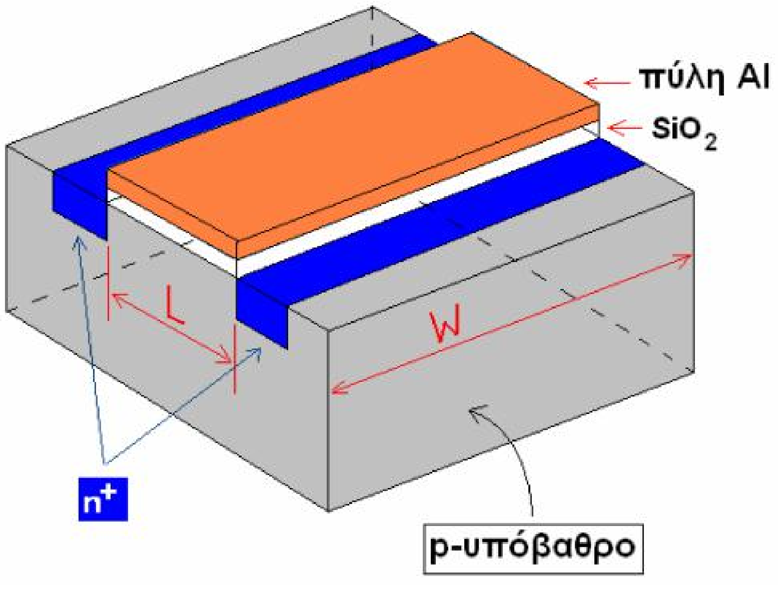
ΕΤΟΣ 2022

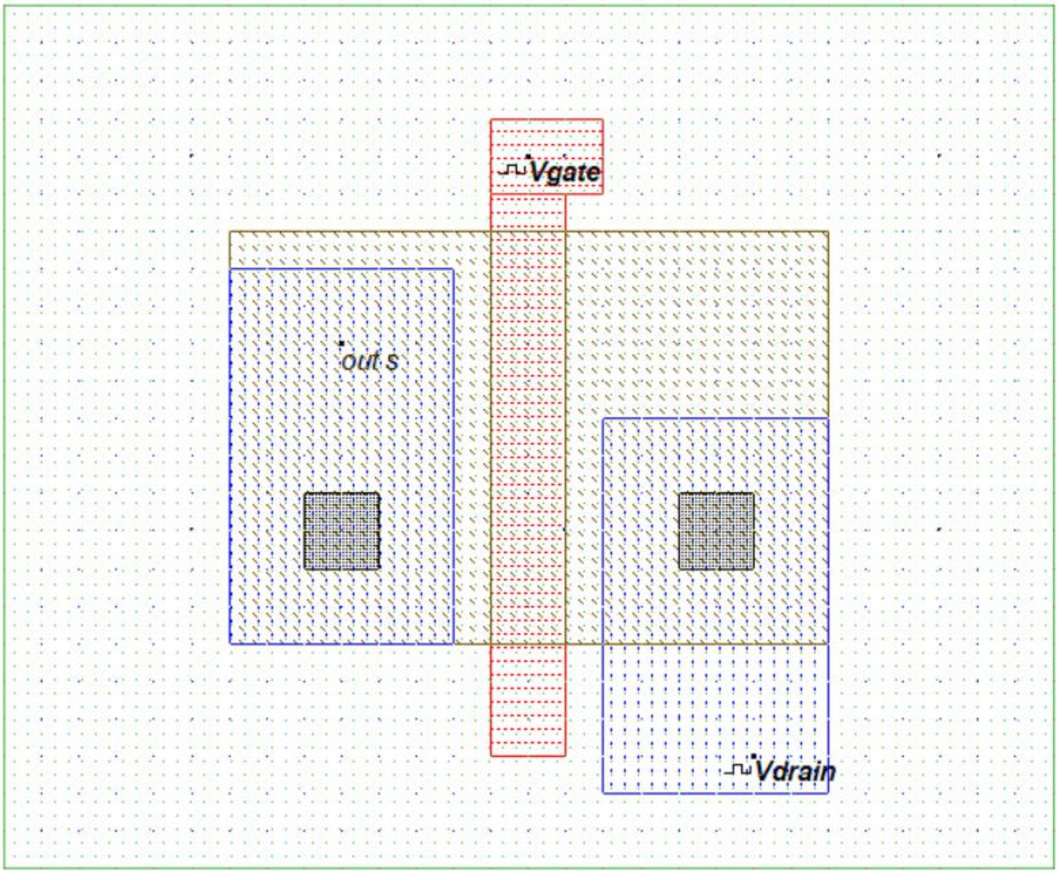
ΑΝΤΩΝΙΟΣ ΜΙΧ. ΜΑΡΑΓΚΟΥΔΑΚΗΣ

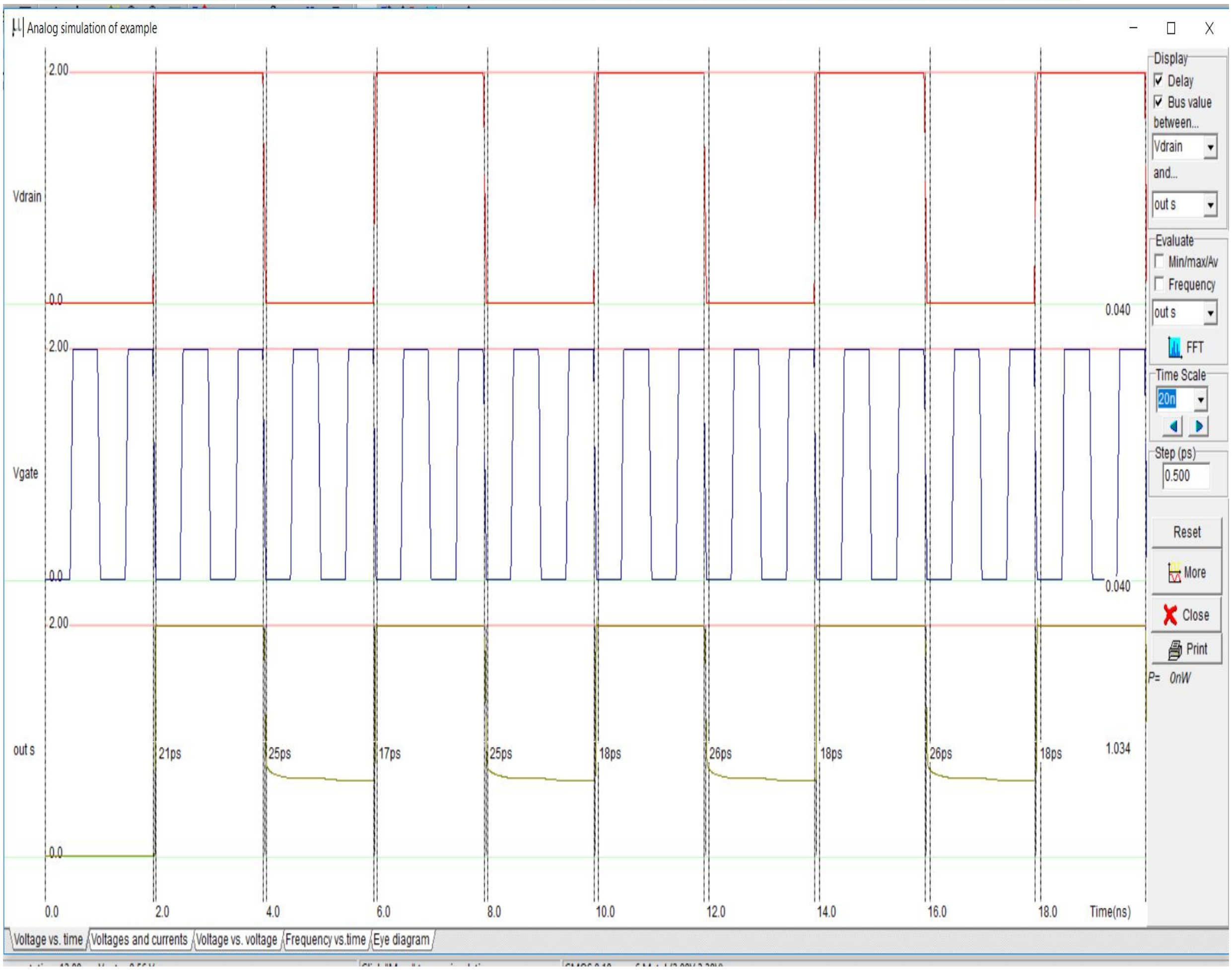


n-type
Open when voltage at G is low
Closed when voltage at G is high

p-type
Closed when voltage at G is low
Open when voltage at G is high







Display
☑ Delay
☑ Bus value
between... Vdrain
and... out s

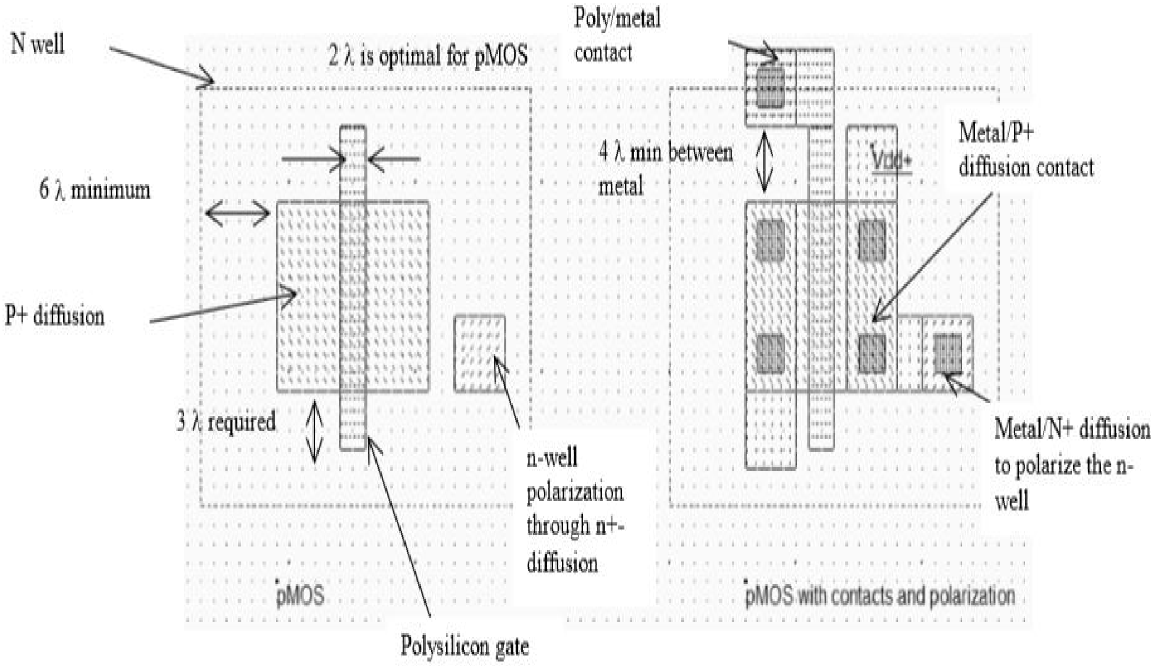
Evaluate
☐ Min/max/Av
☐ Frequency
out s

Time Scale 20n

Step (ps) 0.500

P= 0nW

Χωρίς πόλωση n - πηγαδιού (well) εμφανίζει παρασιτικά φαινόμενα , σαν μια παρασιτική συσκευή PNP.Μια απευθείας τάση Vdd πάνω στο Drain μπορεί να καταστρέψει το κύκλωμα. Με σωστή τάση πηγαδιού n+ - well Vdd σε μια επαφή n+ well στην περιοχή του πηγαδιού n - well αποφεύγονται τα παρασιτικά φαινόμενα.



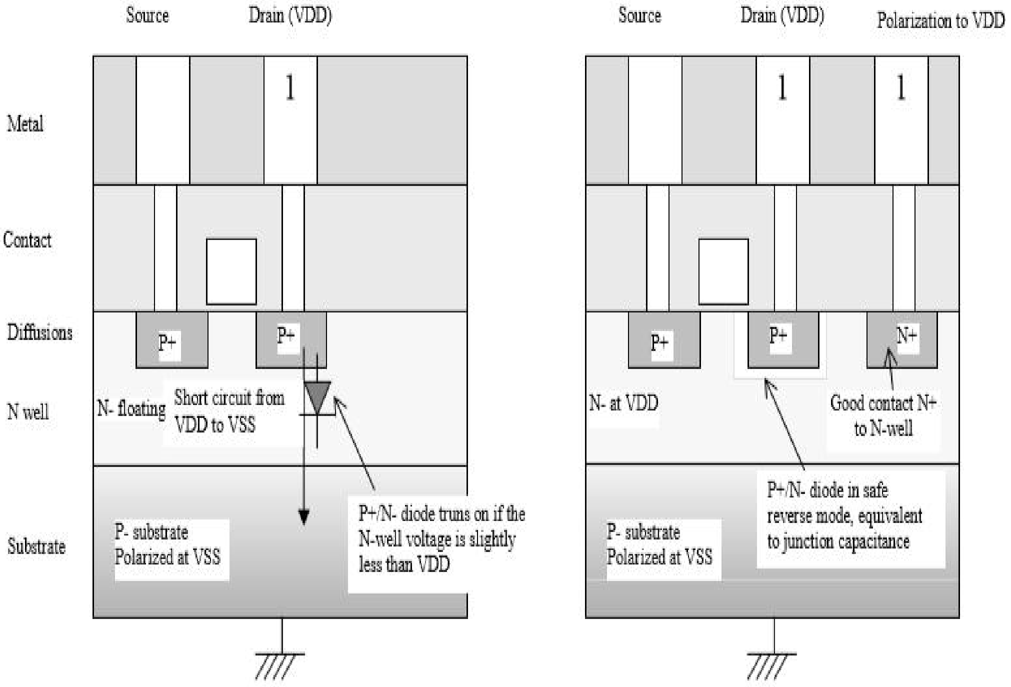
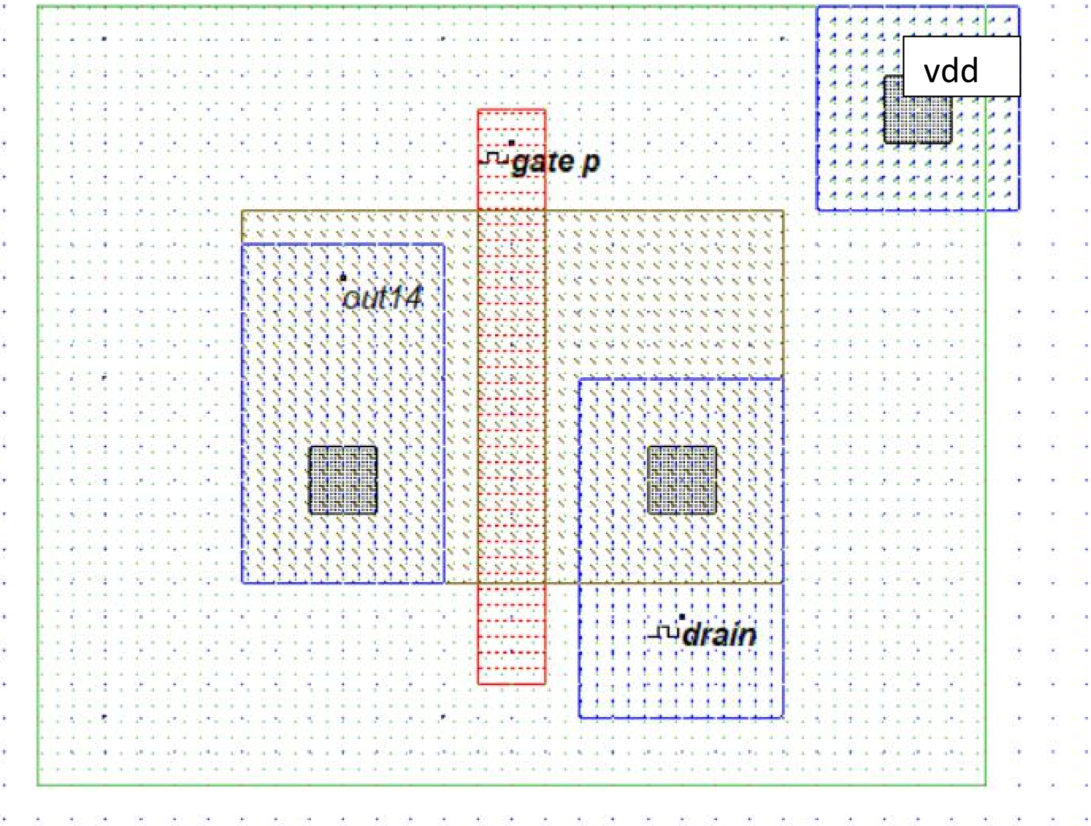
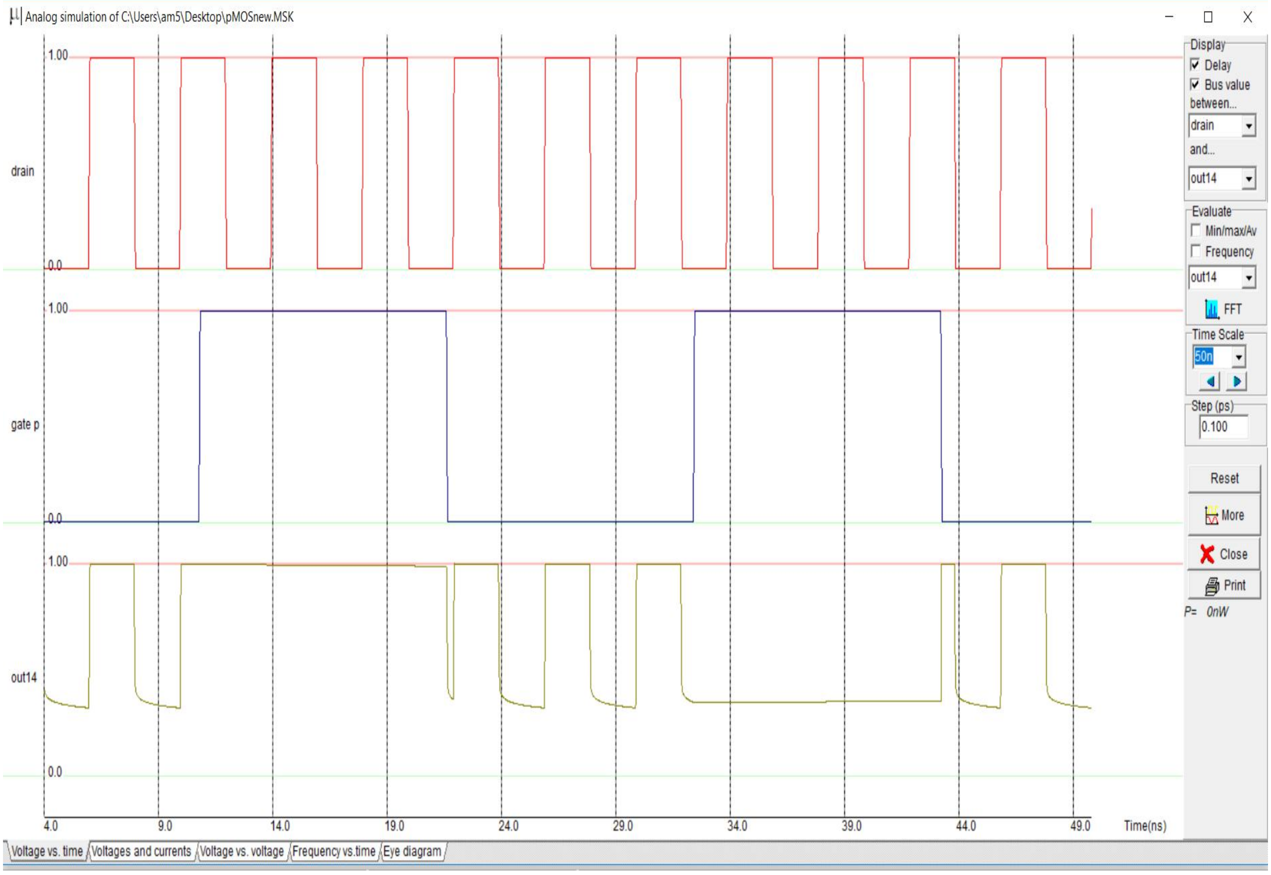


Fig. . Incorrect and correct polarization of the N-well




Analog simulation of C:\Users\am5\Desktop\pMOSnew.MSK

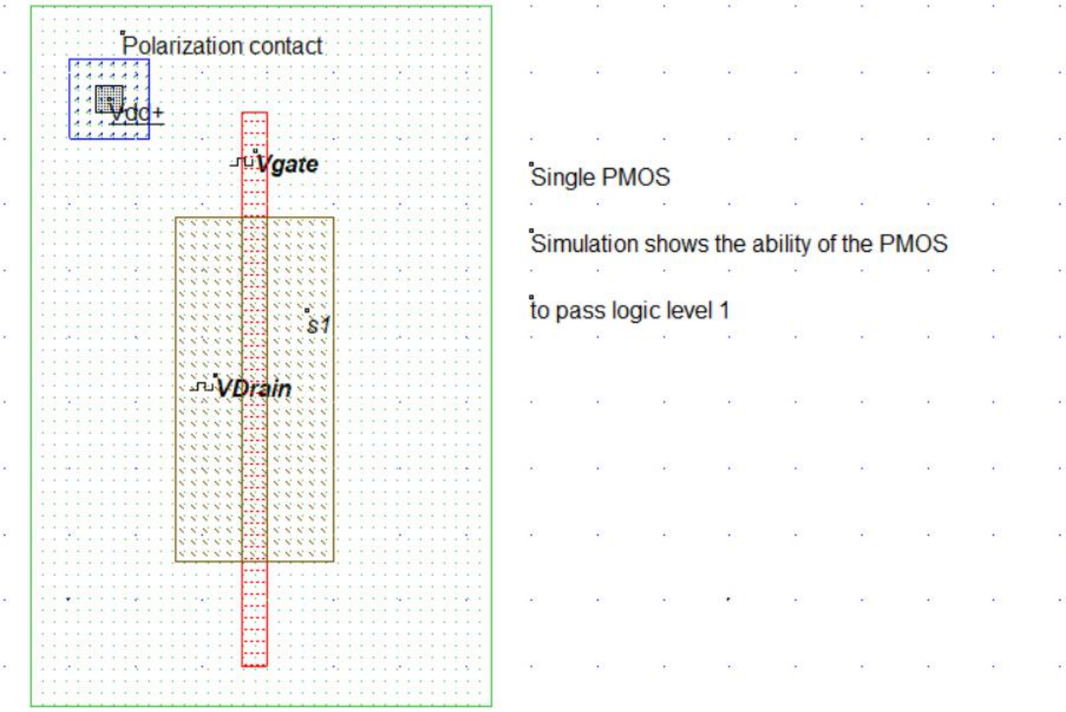
Display
☑ Delay
☑ Bus value
between... drain
and... out14

Evaluate
☐ Min/max/Av
☐ Frequency
out14

Time Scale 50n

Step (ps) 0.100

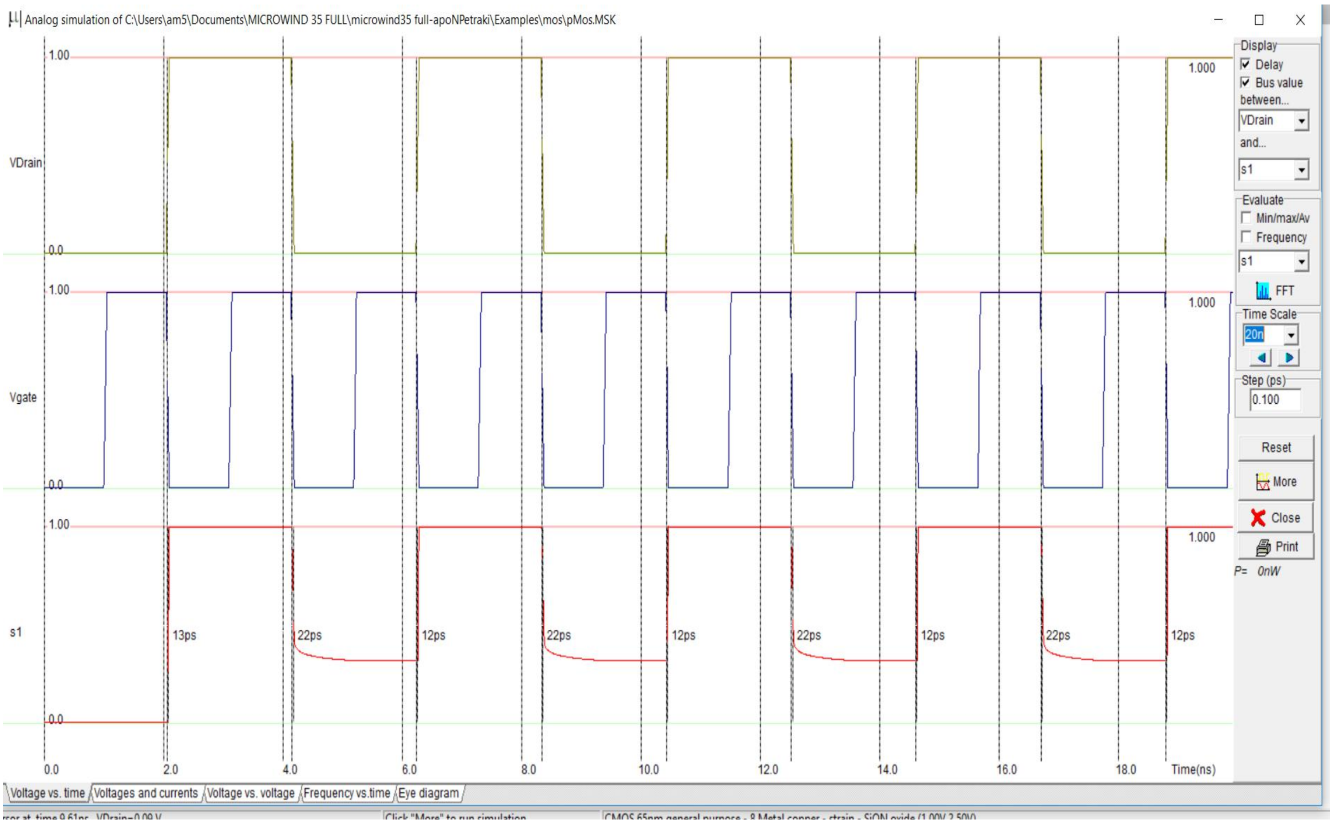
P= 0nW



Single PMOS

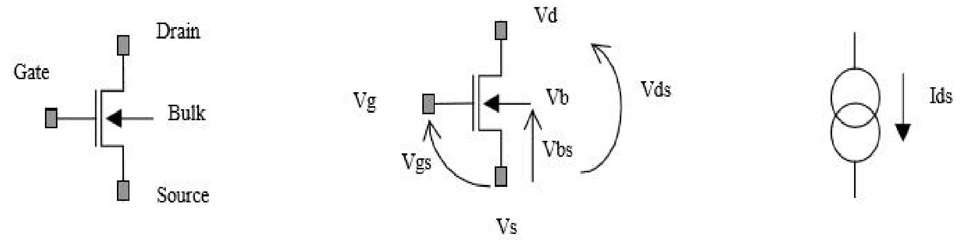
Simulation shows the ability of the PMOS

to pass logic level 1

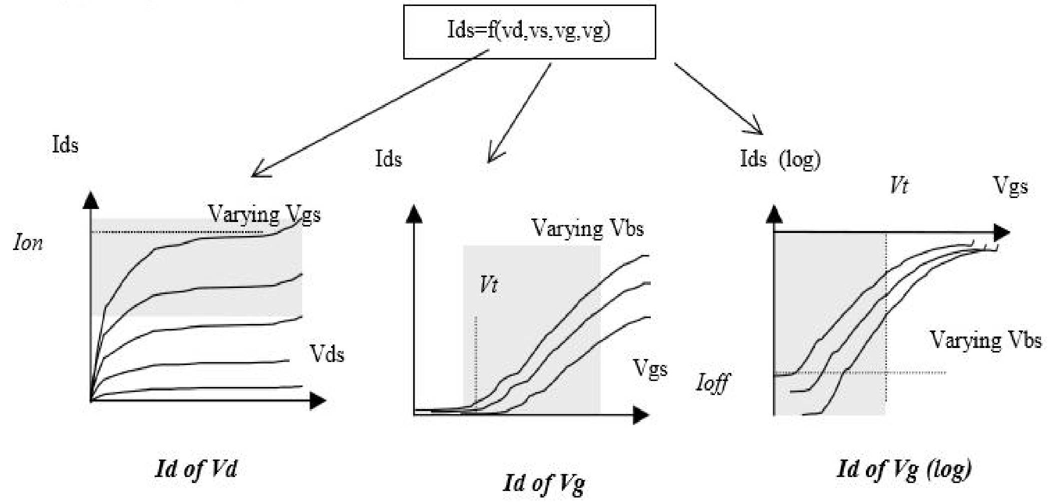


Analog simulation of C:\Users\am5\Documents\MICROWIND 35 FULL\microwind35 full-apoNPetraki\Examples\mos\pMos.MSK

```
rsor at time 9.61ns VDrain=0.09 V
Click "More" to run simulation
CMOS 65nm general purpose - 8 Metal copper - strain - SiON oxide (1.00V 2.50V)
```



$$Ids = f(Vd,Vg,Vs,Vb) \qquad \text{(eq 3-1)}$$



Id of Vd

Id of Vg

Id of Vg (log)

Figure Useful representations of the MOS device characteristics

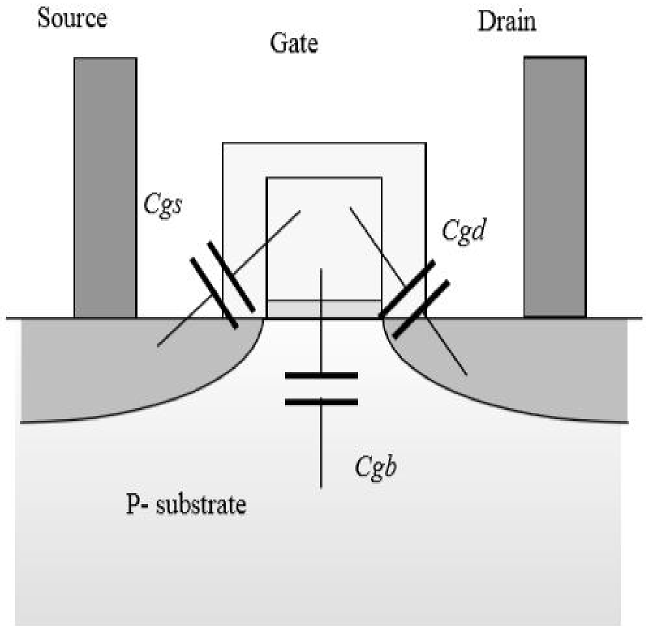


Figure : Capacitance between the gate and the source, drain, or substrate

$$Cgs = f_1(Vd,Vg,Vs,Vb) \qquad \text{(eq 3-2)}$$

$$Cgd = f_2(Vd,Vg,Vs,Vb) \qquad \text{(eq 3-3)}$$

$$Cgb = f3(Vd,Vg,Vs,Vb) \qquad \text{(eq 3-4)}$$

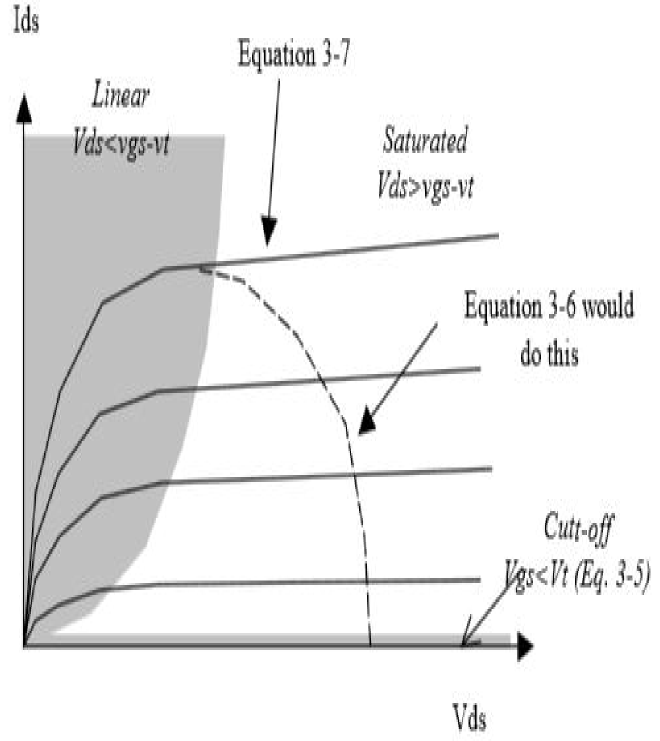


Figure . Two main domains are considered in the model: the linear area and the saturated area.

Το μοντέλο 1 MOS Model 1 είναι το απλό μοντέλο, το μοντέλο 3 MOS Model 3 στους υπολογισμούς λαμβάνει υπόψην ένα σύνολο απο φυσικούς περιορισμούς με κάποιον ημι - εμπειρικό τρόπο. Στο μοντέλο BSIM4 υποστηρίζει τεχνολογία εξαιρετικά λίγων μικρών , υποστηρίζει τις τρεις (3) περιοχές λειτουργίας: γραμμική, κόρου,και κάτω απο το κατώφλι Vgs< Vt και παρέχει μια τέλεια συνέχεια μεταξύ των περιοχών, εισάγει μια νέα περιοχή όπου κυριαρχεί το φαινόμενο της σύγκρουσης των ιόντων. Επίσης υποστηρίζει γύρω στους 300 παραμέτρους. Εμείς χρησιμοποιούμε γύρω στους 20.

IF $V_{gs}<0$, the device is in cut-off mode.

$$Ids = 0 \tag{3-5}$$

IF $V_{ds}<V_{gs}$-VTO, the device is in linear mode

$$Ids = \mathrm{UO}\frac{\varepsilon_0 \varepsilon_r}{\mathrm{TOX}}.\frac{\mathrm{W}}{\mathrm{L}}((V_{gs} - vt).V_{ds} - \frac{(V_{ds})^2}{2})) \tag{3-6}$$

IF $V_{ds}>V_{gs}$-VTO, the device is in saturated mode:

$$Ids = \mathrm{UO}\frac{\varepsilon_0 \varepsilon_r}{\mathrm{TOX}}.\frac{\mathrm{W}}{\mathrm{L}}(V_{gs} - vt)^2 \tag{3-7}$$

With:

$$vt = \mathrm{VTO} + \mathrm{GAMMA}(\sqrt{(\mathrm{PHI} - vbs)} - \sqrt{\mathrm{PHI}}) \tag{3-8}$$

$\varepsilon_0 = 8.85\ 10^{-12}$ F/m is the absolute permittivity

ε_r = relative permittivity, equal to 3.9 in the case of SiO2 (no unit)

Mos Model 1 parameters			
Parameter	Definition	Typical Value 0.12µm NMOS	 PMOS
`VTO`	Theshold voltage	0.4V	-0.4V
`U0`	Carrier mobility	$0.06\mathrm{m}^2$/V-s	$0.02\mathrm{m}^2$/V-s
`TOX`	Gate oxide thickness	2nm	2nm
`PHI`	Surface potential at strong inversion	0.3V	0.3V
`GAMMA`	Bulk threshold parameter	$0.4\ \mathrm{V}^{0.5}$	$0.4\ \mathrm{V}^{0.5}$
`W`	MOS channel width	1µm	1µm
`L`	MOS channel length	0.12µm	0.12µm

Table : Parameters of MOS level 1 implemented into Microwind2

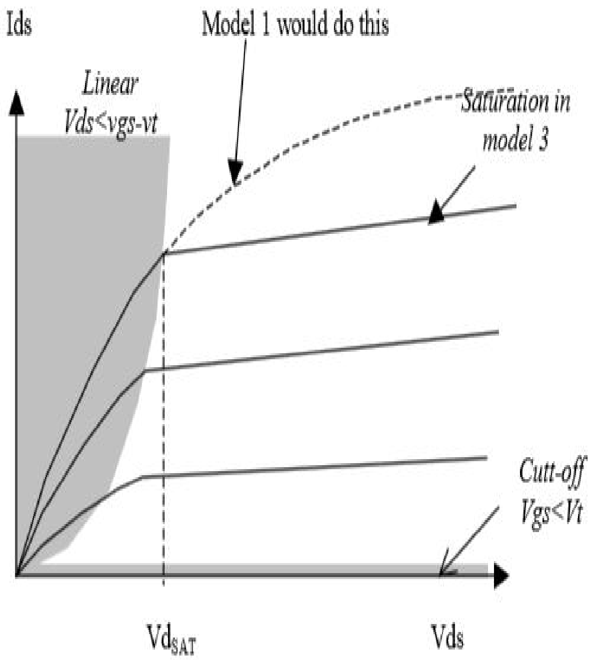


Figure Introduction of the saturation voltage VdSat which truncates the equations issued from model 1

One of the most important change is the introduction of Vd_{SAT}, a saturation voltage from which the current saturates and do not rise as the LEVEL1 model would do. This saturation effect is significant for small channel length. The main LEVEL3 equations are listed below.

CUT-OFF MODE. Vgs<0

$$Ids = 0 \qquad (3\text{-}9)$$

NORMAL MODE. Vgs>Von

$$Ids = Keff\,\frac{W}{Leff}(1+\mathrm{KAPPA}.Vds)Vde((Vgs - Vth) - \frac{Vde}{2}) \qquad (3\text{-}10)$$

with

$$Von = 1.2Vth$$

$$Vth = \mathrm{VTO} + \mathrm{GAMMA}(\sqrt{\mathrm{PHI} - Vbs} - \sqrt{\mathrm{PHI}})$$

$$Vde = min(Vds, Vdsat)$$

$$Vdsat = Vc + Vsat - \sqrt{Vc^2 + Vsat^2}$$

$$Vdsat = Vgs - Vth$$

$$Vc = \mathrm{VMAX}\frac{Leff}{0.06}$$

$$Leff = L - 2LD$$

The formulation of the effective factor *Keff* (Equation 3-11) includes a mobility degradation factor `THETA`, which tends to reduce the mobility at high *Vgs*. The consequence is a reduction of the current Ids as compared to LEVEL1.

$$Keff = \frac{\varepsilon_0 \varepsilon_r}{\mathrm{TOX}} \frac{\mathrm{UO}}{(1 + \mathrm{THETA}(vgs - vth))} \qquad (3\text{-}11)$$

In sub-threshold mode, that is for a gate voltage less than the threshold voltage, *Vds* is replaced by *Von* in the above equations. An exponential dependence of the current with *Vgs* is introduced by using the equation 3-12. Notice the temperature effect introduced in the denominator *nkT*.

Without any voltage applied to the gate, the current is no more equal to zero. The current of *Ids* for *Vgs*=0 is called the *Ioff* current (Figure 3-9). Its value in 0.12µm is around 10^{-10} A. In contrast, for *Vgs*=VDD, the maximum current *Ion* is of the order of several mA (10^{-3} A).

$$Ids = Ids(Von,Vds)exp(\frac{q(Vgs - Von)}{nkT}) \quad (3\text{-}12)$$

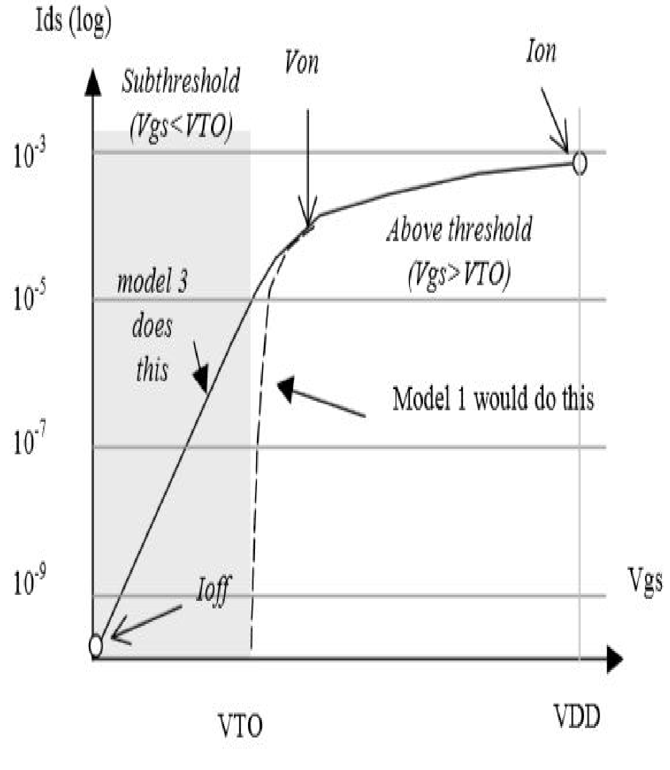


Figure 3-9: Introduction of an exponential law to model the sub-threshold behavior of the current

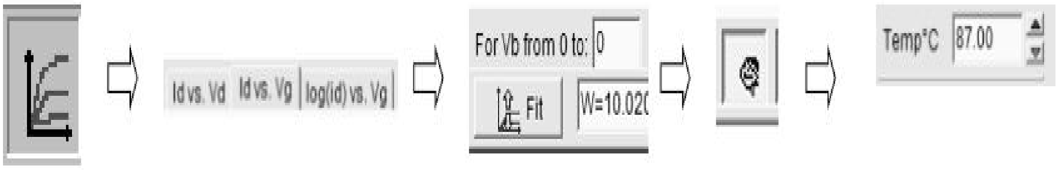
Επιδράσεις απο την θερμοκρασία

The MOS device is sensitive to temperature. Three main parameters are concerned: the threshold voltage `VTO`, the mobility `U0` and the slope in sub-threshold mode dependent on *kT/q*. Both `VTO` and `U0` decrease when the temperature increases . The physical background is the degradation of the mobility of electrons

and holes when the temperature increase, due to a higher atomic volume of the crystal underneath the gate, and consequently less space for the current carriers. The modeling of the temperature effect is as follows:

$$\mathrm{U0} = \mathrm{U0}_{(\mathrm{T}=27)}\left(\frac{\mathrm{T}+273}{300}\right)^{-1.5} \qquad \text{(eq. 3-13)}$$

$$\mathrm{VT} = \mathrm{VT0}_{(\mathrm{T}=27)} - 0.002(\mathrm{T}-300) \qquad \text{(eq. 3-14)}$$



Mos characteristics

Select Id/Vg

Only one curve (Vb=0)

Ask for memory effect

Modify temperature

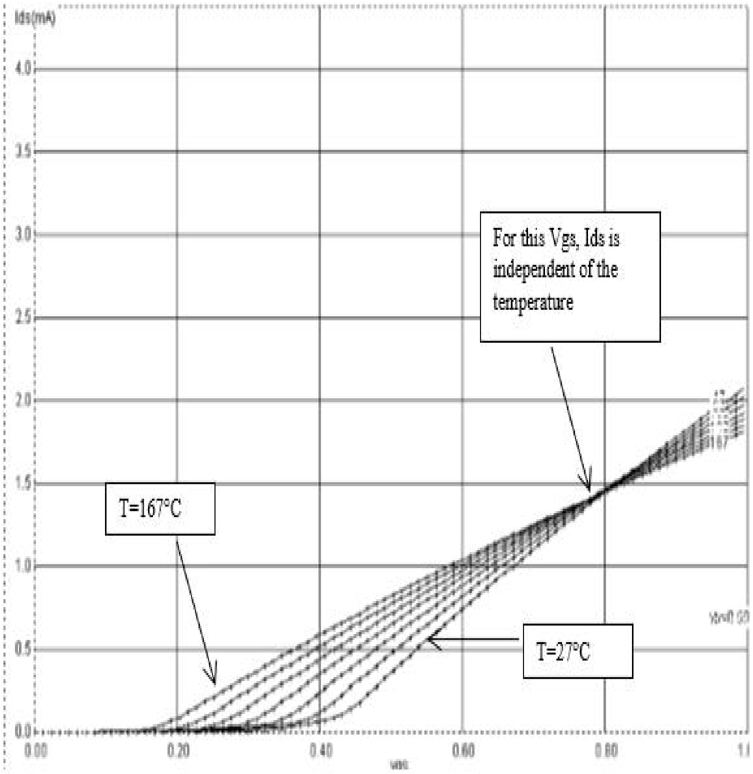


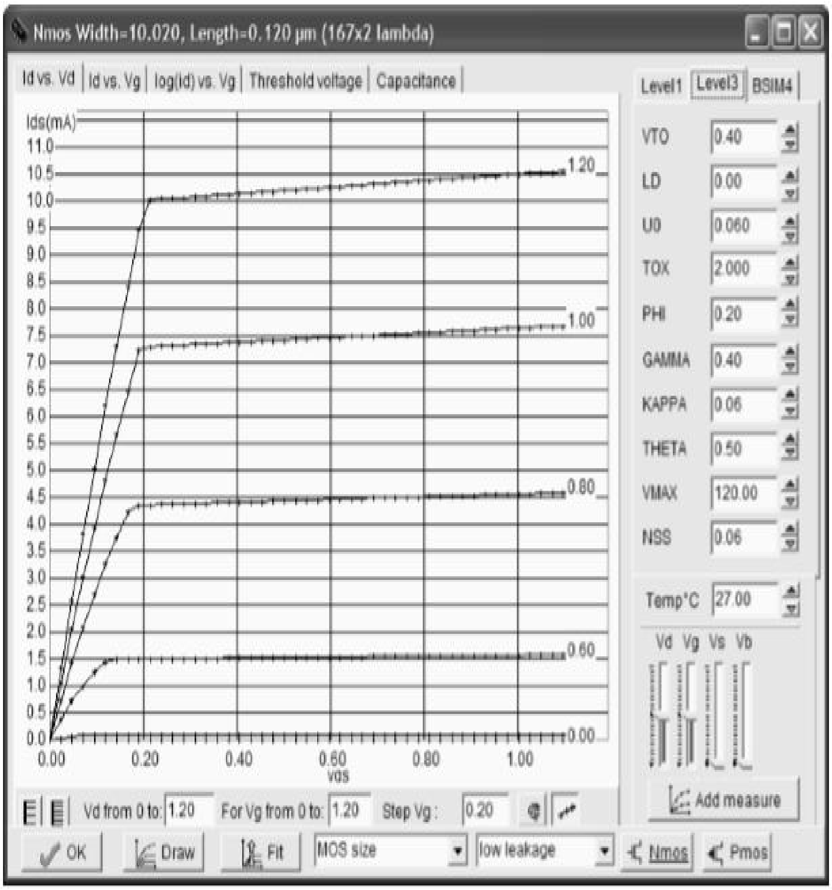
Figure 3-10 The effect of temperature on the MOS characteristics. In Id/Vg mode, a specific Vds makes the current independent of the temperature.

To obtain the curve of figure 3-10, click the icon MOS characteristics, select the curve *Id/Vg*, and enter the value "0" for the upper limit of *Vb*, so as to draw only one single curve. Enable the screen memory mode by a click on the icon **Enable Memory**. When you change the temperature, the change in the slope and the temperature-independent point appear, as shown in figure 3-10.

Mos Model 3 parameters			
Parameter	Definition	Typical Value 0.12µm NMOS	 pMOS
VTO	Theshold voltage of a long channel device, at zero Vbs.	0.4V	-0.4V
U0	Carrier mobility	0.06 m^2/V.s	0.025 m^2/V.s
TOX	Gate oxide thickness	3 nm	3 nm
PHI	Surface potential at strong inversion	0.3V	0.3V

LD	Lateral diffusion into channel	0.01µm	0.01µm
GAMMA	Bulk threshold parameter	0.4 $V^{0.5}$	0.4 $V^{0.5}$
KAPPA	Saturation field factor	0.01 V^{-1}	0.01 V^{-1}
VMAX	Maximum drift velocity	150Km/s	100Km/s
THETA	Mobility degradation factor	0.3 V^{-1}	0.3 V^{-1}
NSS	Substhreshold factor	0.07 V^{-1}	0.07 V^{-1}
W	MOS channel width	0.5-20µm	0.5-40µm
L	MOS channel length	0.12µm	0.12µm

Table 3-xxx: list of parameters used in the implementation of the LEVEL3 model in Microwind2

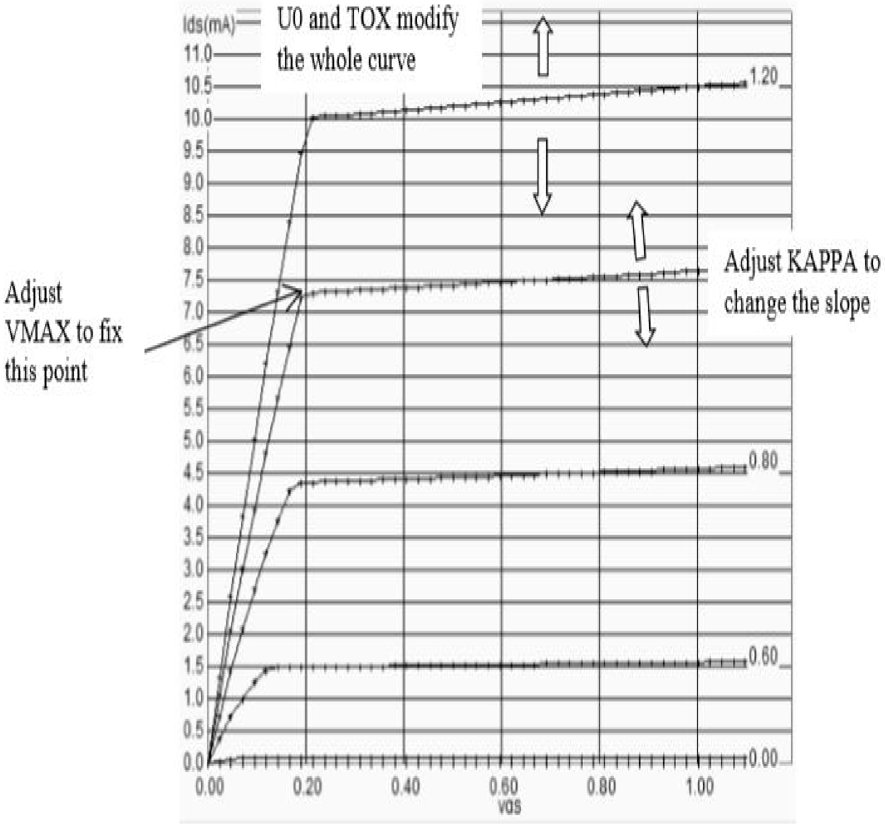


Nmos Width=10.020, Length=0.120 µm (167x2 lambda)

VTO 0.40
LD 0.00
U0 0.060
TOX 2.000
PHI 0.20
GAMMA 0.40
KAPPA 0.06
THETA 0.50
VMAX 120.00
NSS 0.06
Temp°C 27.00

Vd from 0 to: 1.20
For Vg from 0 to: 1.20
Step Vg : 0.20
MOS size
low leakage

Fig. 3-11. The user interface to investigate the effect of each parameter on the current Ids (W=10µm, L=0.12µm)

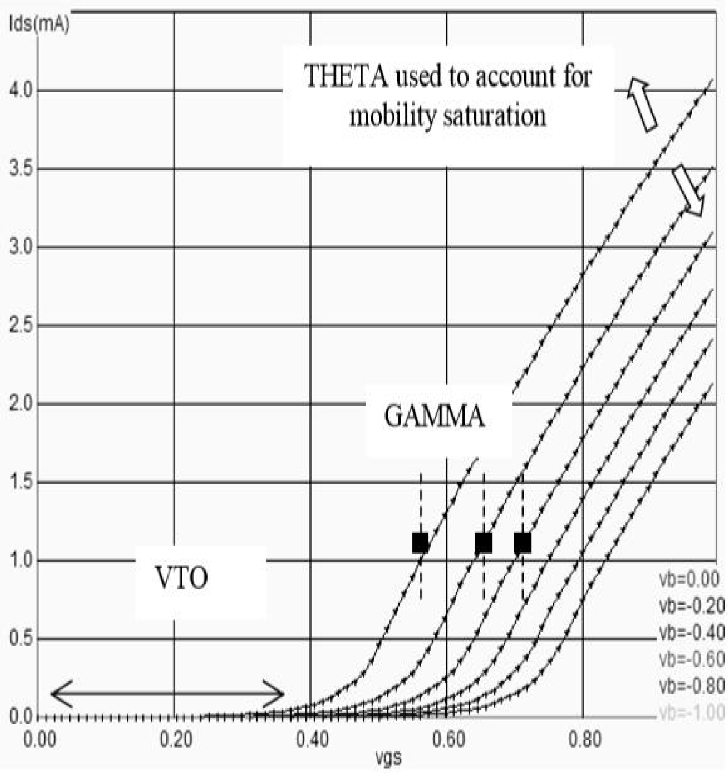


U0 and TOX modify the whole curve

Adjust KAPPA to change the slope

Adjust VMAX to fix this point

Fig. 3-12. Demonstration of the role of U0, KAPPA and VMAX in Id./Vd (W=10µm, L=0.12µm)



THETA used to account for mobility saturation

GAMMA

VTO

Fig. 3-13. The effects of VTO and GAMMA are illustrated in Id/Vg mode voltage (W=10µm, L=0.12µm)

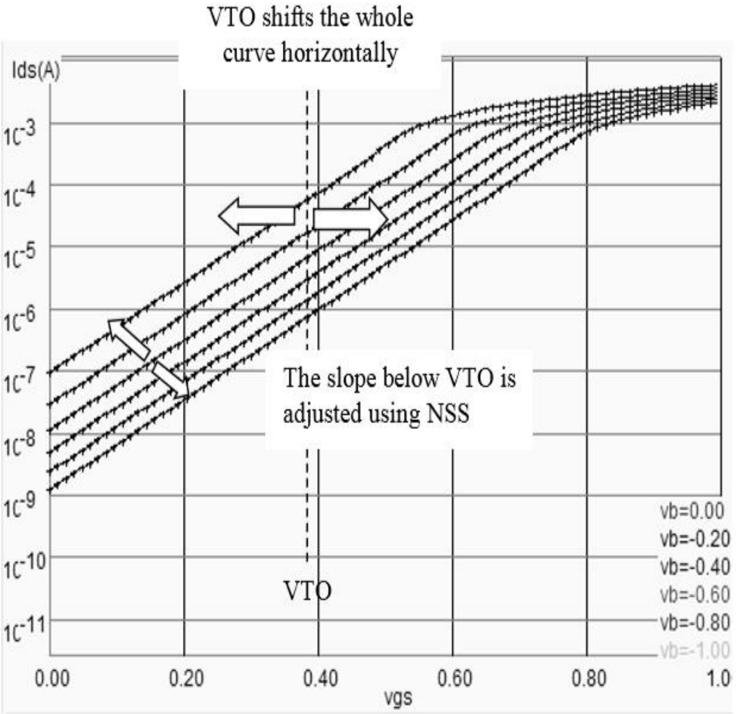


Figure 3-14. In sub-threshold region, the Id dependence on Vgs is exponential. The slope is tuned by parameter NSS. The whole curve is shifted using VTO voltage (W=10µm, L=0.12µm)

Capacitance vs. Vds

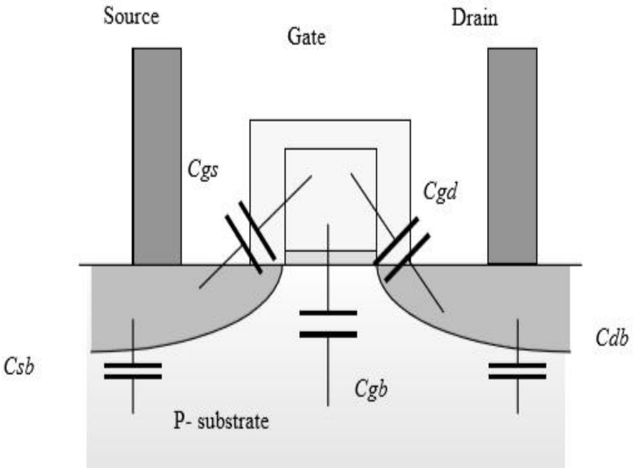


Figure 3-15: The MOS capacitance considered in MOS model 3

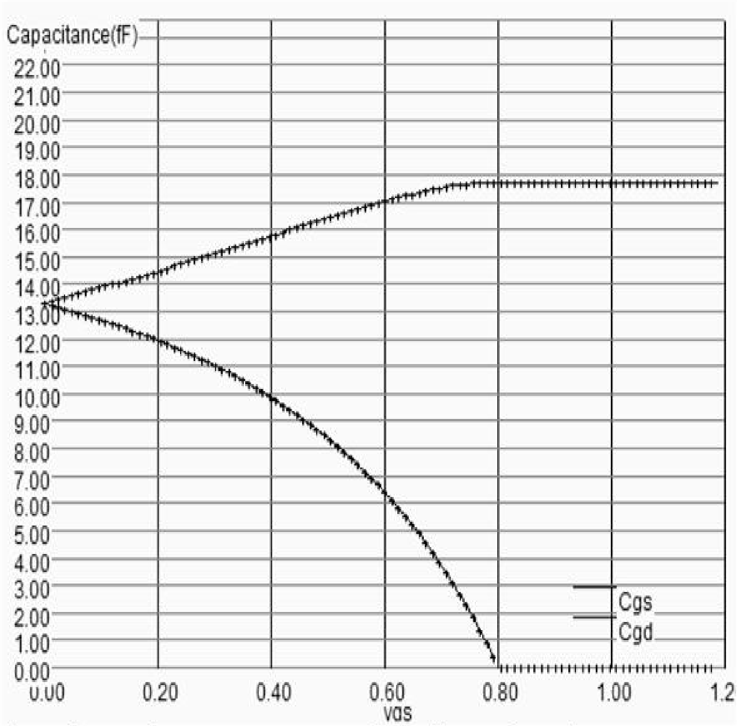


Figure 3-16: The evolution of MOS capacitance with the drain voltage (W=10µm, L=0.12µm)

$$C_{GS} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GS} - V_t - V_{dsat}}{2(V_{GS} - V_t) - V_{dsat}} \right)^2 \right] \tag{3-15}$$

$$C_{GD} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GS} - V_t}{2(V_{GS} - V_t) - V_{dsat}} \right)^2 \right] \tag{3-16}$$

$$C_{GB} = 0 \tag{3-17}$$

with

$$Ci = W.L.\frac{\varepsilon_0 \varepsilon_r}{\mathrm{TOX}} \tag{3-18}$$

W = width of the MOS device (m)

L = length of the MOS device (m)

TOX = oxide thickness (m)

The two remaining capacitance C_{DB} and C_{SB} are junction capacitance. Their model is given by equations 3-19 and 3-20.

$$C_{DB} = W.L_{drain} \frac{\mathrm{CJ}}{\left(1 - \frac{V_{BD}}{\mathrm{PB}}\right)^{\mathrm{MJ}}} \tag{3-19}$$

$$C_{SB} = W.L_{source} \frac{\mathrm{CJ}}{\left(1 - \frac{V_{BS}}{\mathrm{PB}}\right)^{\mathrm{MJ}}} \tag{3-20}$$

where

W is the channel width (m)

L_{drain} is the drain length, according to figure 3-17 (m)

CJ is around 3x10e-4 F/m2

PB is the built-in potential of the junction (around 0.8V)

MJ is the grading coefficient of the junction (around 0.5)

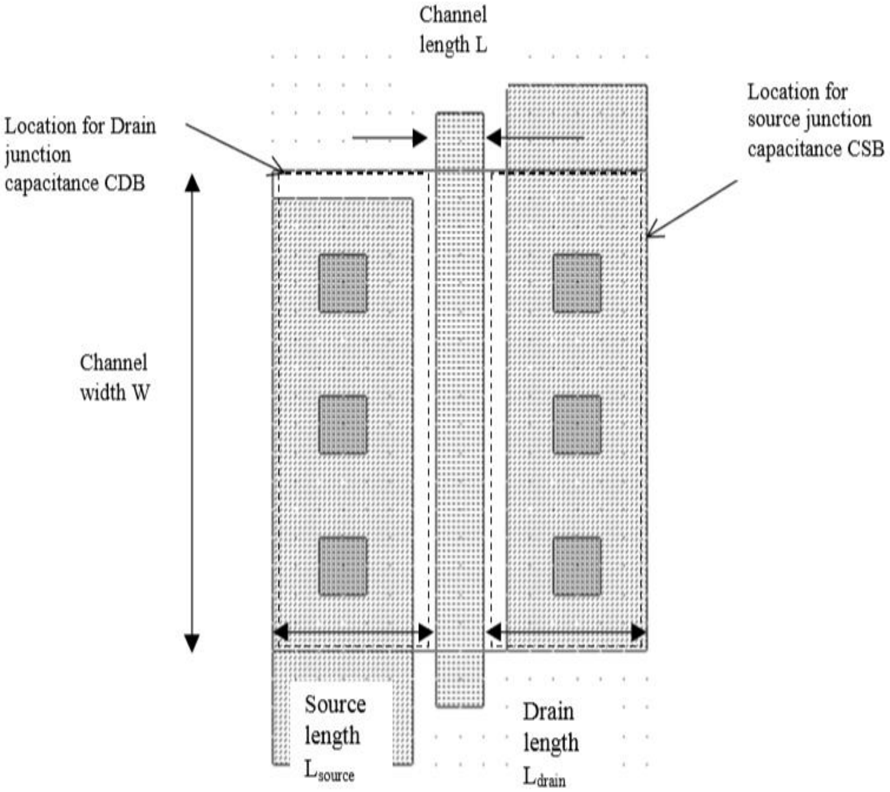


Figure 3-17: The junction capacitance for drain and source contributes significantly to the MOS capacitance

BSIM4 MODEL

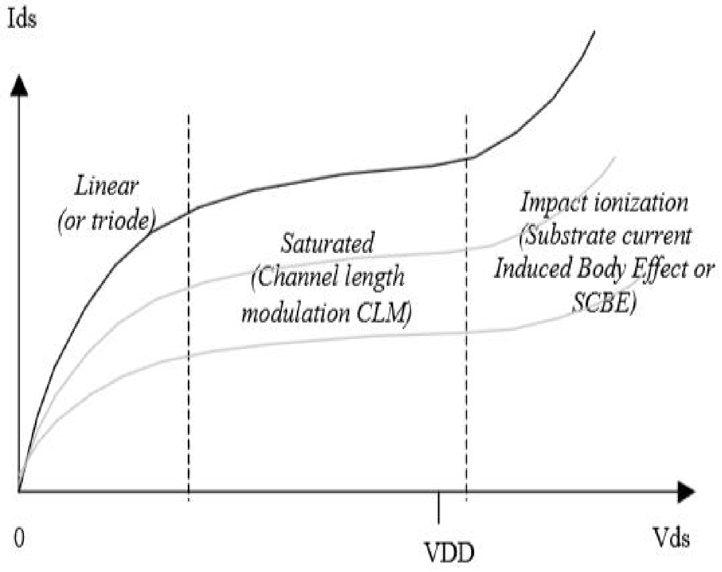


Figure The three regions considered in our simplified version of BSIM4

ΠΗΓΉ : MICROWIND
: Etienne Sicard