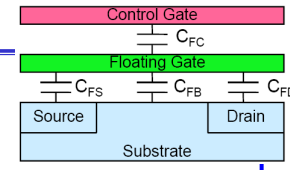
Μικροηλεκτρονική & VLSI



Μάθημα 13:

Τεχνολογίες Μνήμης MOS

Λευτέρης Καπετανάκης

Ελληνικό Μεσογειακό Πανεπιστήμιο
Τμήμα Ηλεκτρονικών Μηχανικών
2021-2022

Slide 1

ΣΗΜΕΙΩΣΗ: Στις διαφάνειες των διαλέξεων χρησιμοποιείται διδακτικό υλικό το οποίο έχει δανειστεί από διάφορα εκπαιδευτικά βιβλία και διαδικτυακές σελίδες. Ο εισηγητής δεν έχει καμιά αξίωση κατοχής του υλικού αυτού και το χρησιμοποιεί μόνο για λόγους διδασκαλίας εντός της τάξης. Οι εικόνες και οι πίνακες είναι κτήμα διαφόρων συγγραφέων και παρέχονται στον αντίστοιχο δικτυότοπό τους.

Slide 2

Χαρακτηριστικά του "ιδανικού", καθολικής χρήσης, τσιπ μνήμης:

φτηνό στην κατασκευή του

ικανό να συγκρατεί το περιεχόμενό του όταν διακόπτεται η παροχή τροφοδοσίας

τυχαία προσπελάσιμο με δυνατότητα γρήγορης ανάγνωσης /εγγραφής των δεδομένων

χαμηλής κατανάλωσης ισχύος

μεγάλης πυκνότητας

υψηλής αξιοπιστίας

εύκολο στον έλεγχο της λειτουργίας του

συμβατό με τις συνήθεις βιομηχανικές διαδικασίες κατασκευής.

Δυστυχώς, μια ξεχωριστή διάταξη μνήμης η οποία να έχει όλα αυτά τα χαρακτηριστικά δεν είναι εφικτή μέχρι σήμερα

Εισαγωγικές έννοιες

Με βάση την τεχνολογία κατασκευής τους, τα εμπορικά μέσα αποθήκευσης μπορούν να χωριστούν σε μνήμες:

ημιαγωγικού τύπου (MOS, BJT, διατάξεις σύζευξης φορτίου CCDs)

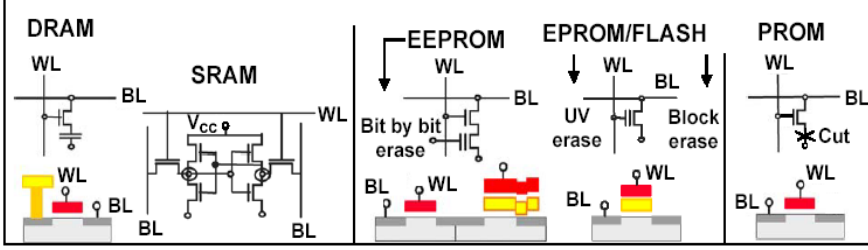
μηχανικού τύπου όπου η αποθήκευση των δεδομένων γίνεται πάνω σε κινούμενες επιφάνειες (μαγνητικοί δίσκοι ή ταινίες, οπτικοί δίσκοι).

Λόγω των μοναδικών πλεονεκτημάτων κατασκευής και ολοκλήρωσης των διατάξεων MOS

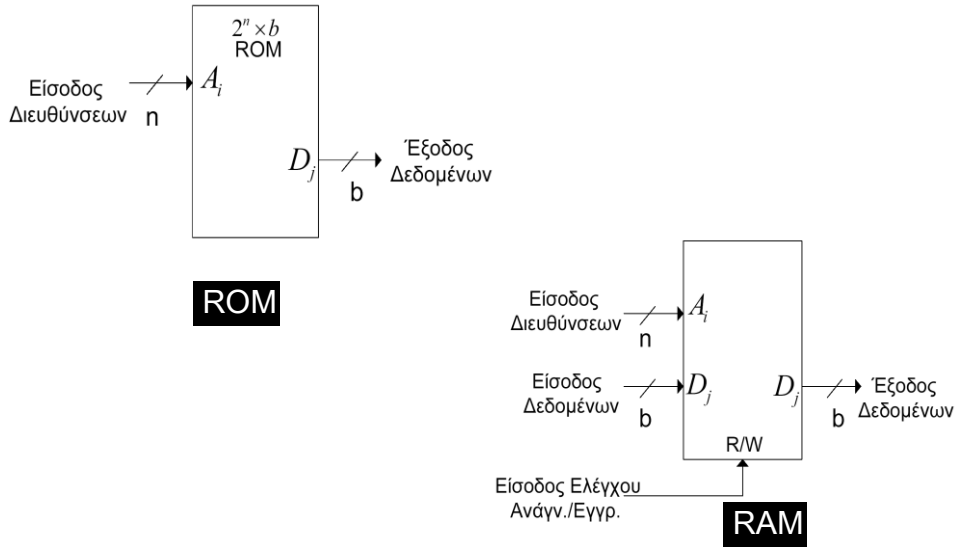
Οι μνήμες MOS αποτελούν σχεδόν την αποκλειστική επιλογή μνήμης των σύγχρονων ηλεκτρονικών συστημάτων, για την αποθήκευση των δεδομένων επεξεργασίας και του κώδικα εκτέλεσης των προγραμμάτων.

ΚΑΤΗΓΟΡΙΕΣ ΗΜΙΑΓΩΓΙΚΗΣ ΜΝΗΜΗΣ ΑΝΑΛΟΓΑ ΜΕ ΤΗΝ:	
Δυνατότητα επαναπρογραμματισμού	**Δυνατότητα συγκράτησης δεδομένων**
Μνήμη Ανάγνωσης Μόνο (Read Only Memory, ROM) Μνήμη Ανάγνωσης/Εγγραφής (Read/Write Memory, RWM)	Μνήμη Μη-Μόνιμης Αποθήκευσης (Volatile Memory) Μνήμη Μόνιμης Αποθήκευσης (Non-Volatile Memory, NVM)

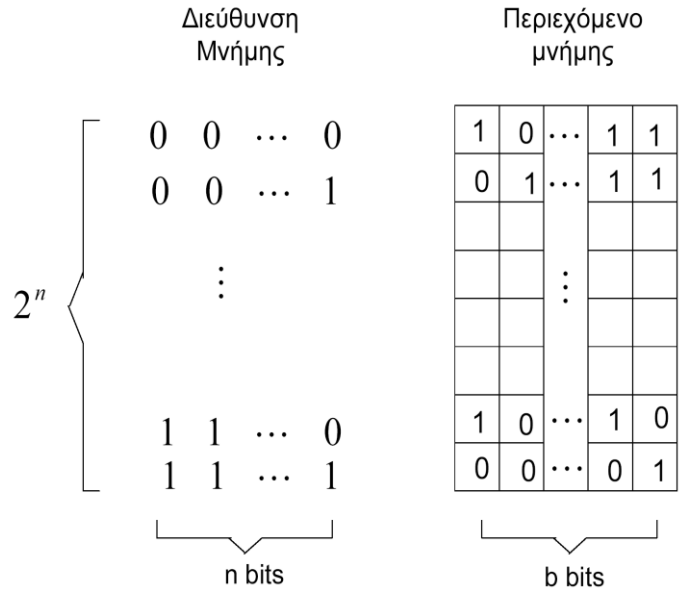
ΤΥΠΟΙ ΗΜΙΑΓΩΓΙΚΗΣ ΜΝΗΜΗΣ MOS		
Volatile	**Non-Volatile (NVM)**	
Volatile RWM ***ή*** ***Random Access Memory (RAM)***	***Non-Volatile RWM (NVRWM)***	***ROM***
Dynamic RAM (DRAM) Static RAM (SRAM)	UV Erasable PROM (EPROM) Electrically Erasable PROM (EEPROM) Flash Memory	Mask-Programmed Programmable (PROM)
Δομή και ισοδύναμο κύκλωμα των κυττάρων της μνήμης MOS		



Σχηματικό διάγραμμα ROM & RAM 2^nxb bits



Λογική διάταξη μνήμης των 2^n λέξεων των b bits



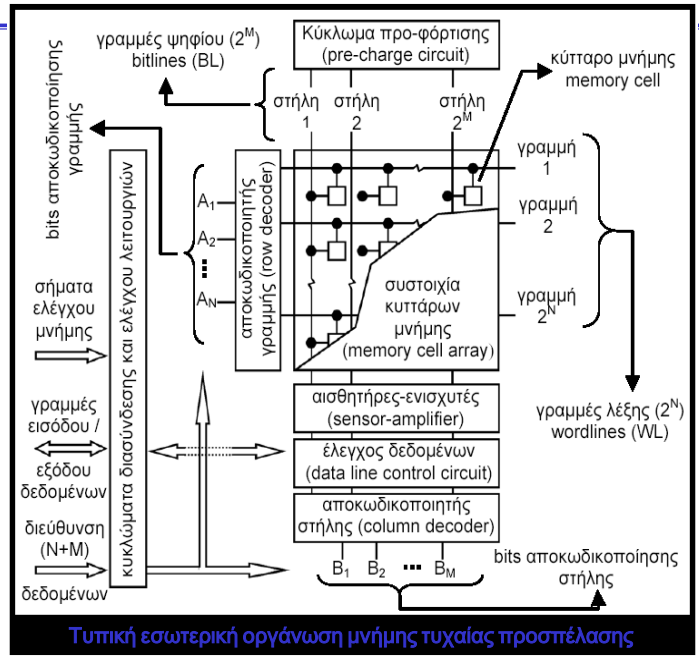
Η μνήμη, ανάλογα με τον τρόπο προσπέλασης των δεδομένων, χωρίζεται σε

σειριακής και τυχαίας προσπέλασης.

Η μνήμη σειριακής προσπέλασης (serial access or sequential access)

δεν έχει σταθερό χρόνο προσπέλασης, αλλά αυτός ποικίλλει ανάλογα με τη θέση στην οποία βρίσκονται τα δεδομένα. Για την ανάγνωση ή εγγραφή ενός δεδομένου σε μια μνήμη σειριακής προσπέλασης, θα πρέπει να διατρέξουμε όλες τις προηγούμενες θέσεις μέχρι να φτάσουμε στην επιθυμητή θέση, όπου βρίσκεται ή πρέπει να βρίσκεται το δεδομένο. Χαρακτηριστικό παράδειγμα μνήμης σειριακής προσπέλασης είναι η μαγνητική ταινία.

Η μνήμη τυχαίας προσπέλασης (random access memory, RAM)
επιτρέπει την ανεξάρτητη (τυχαία) προσπέλαση κάθε θέσης μέσα στη μνήμη, τόσο για ανάγνωση όσο και για εγγραφή δεδομένων.



Τυπική εσωτερική οργάνωση μνήμης τυχαίας προσπέλασης

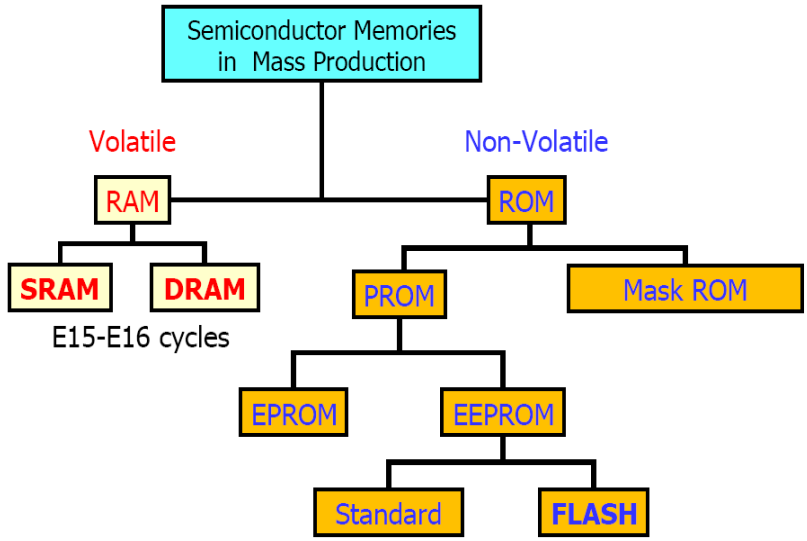
βασική δομή

συστοιχία ή πίνακας κυττάρων μνήμης (*memory cell array or matrix*)

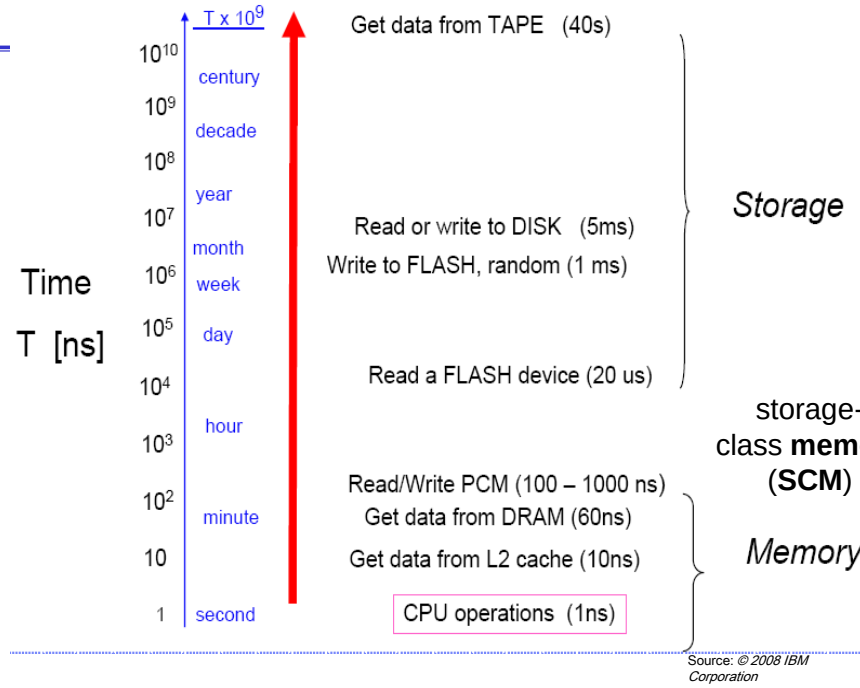
Το κύτταρο της ημιαγωγικής μνήμης είναι ένα ηλεκτρικό κύκλωμα.

Υλοποιείται από μία ή περισσότερες ημιαγωγικές διατάξεις (π.χ. τρανζίστορς, πυκνωτές, αντιστάσεις) και είναι ικανό να αποθηκεύει ένα δυαδικό ψηφίο.

MOSFET Memory



Source: *Pierre Fazan, GSA Memory Conference 2010*



Source: *© 2008 IBM Corporation*

Memory and Logic in a typical computer system

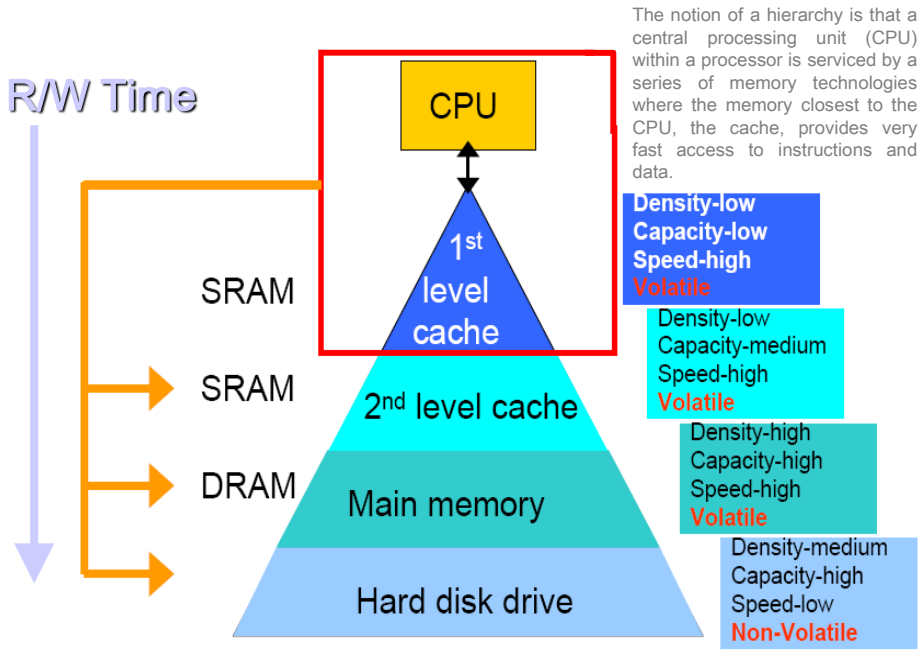
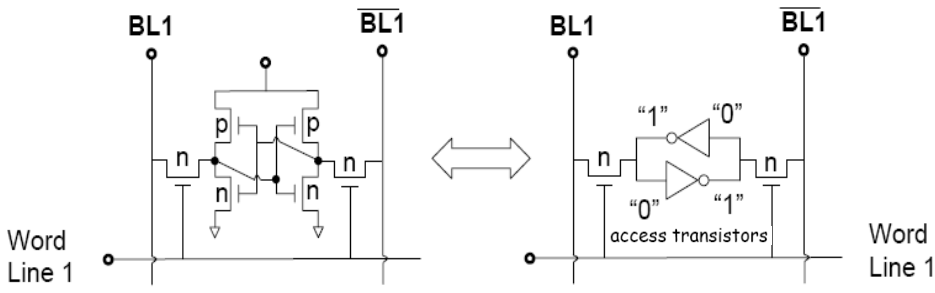


TABLE 6–1 • The differences among three types of memories.

	Keep Data Without Power?	Cell Size and Cost/bit	Rewrite Cycles	Write-One-byte Speed	Compatible with Basic CMOS Manufacturing	Main Applications
SRAM	No	Large	Unlimited	Fast	Totally	Embedded in logic chips
DRAM	No	Small	Unlimited	Fast	Need modifications	Stand-alone chips and embedded
Flash memory	Yes	Smallest	Limited	Slow	Need extensive modifications	Nonvolatile storage stand-alone

Static Random Access Memory (SRAM)

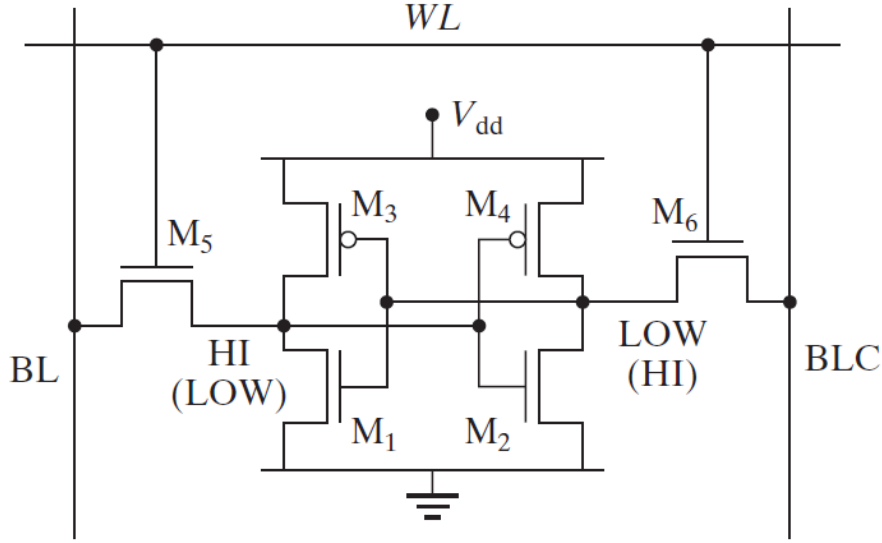


- Static: holds data as long as power is applied
- Volatile: can not hold data if power is removed
- 3 Operation States: hold, write, read

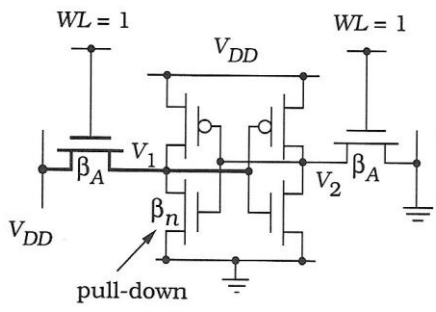
- bistable (cross-coupled) INVs for storage
- word line, WL, controls access
  - WL = 0 (hold) = 1 (read/write)

- **One cell = 6 MOSFETs**
- **Data is stable as long as power is on.**

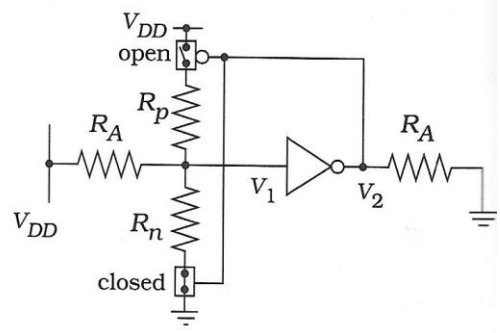
Static RAM is faster than DRAM, also more expensive



Writing to an SRAM



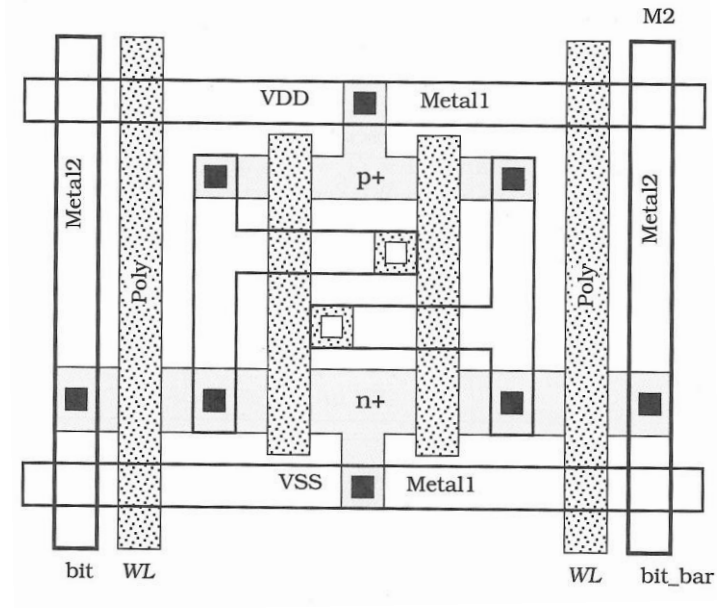
(a) Write 1 operation



(b) Resistor model

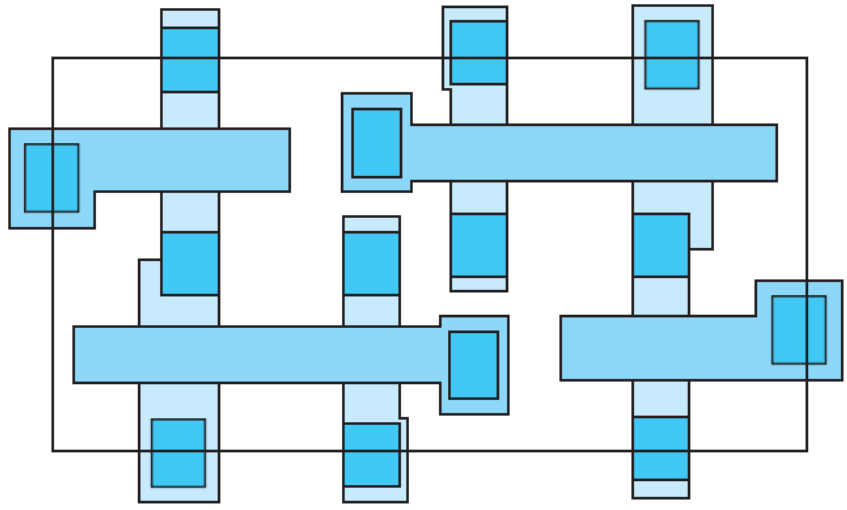
Slide 17

Example of a basic SRAM cell layout



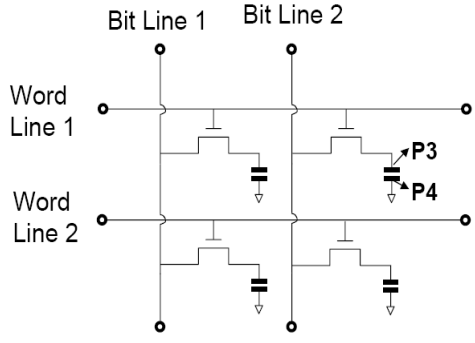
Slide 18

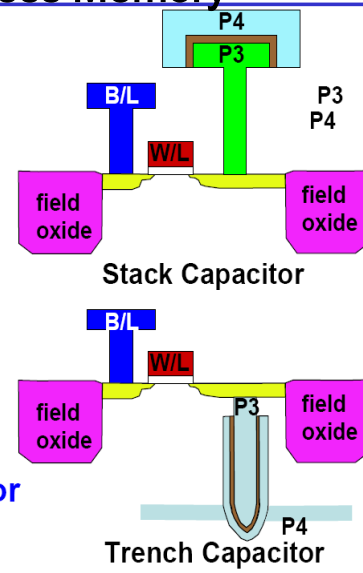
Layout of a 32 nm technology SRAM,



The dark rectangles are the contacts. The four horizontal pieces are the gate electrodes and the two PFETs have larger Ws than the six NFETs. Metal interconnects (not shown) cross couple the two inverters.

Dynamic Random Access Memory (DRAM)

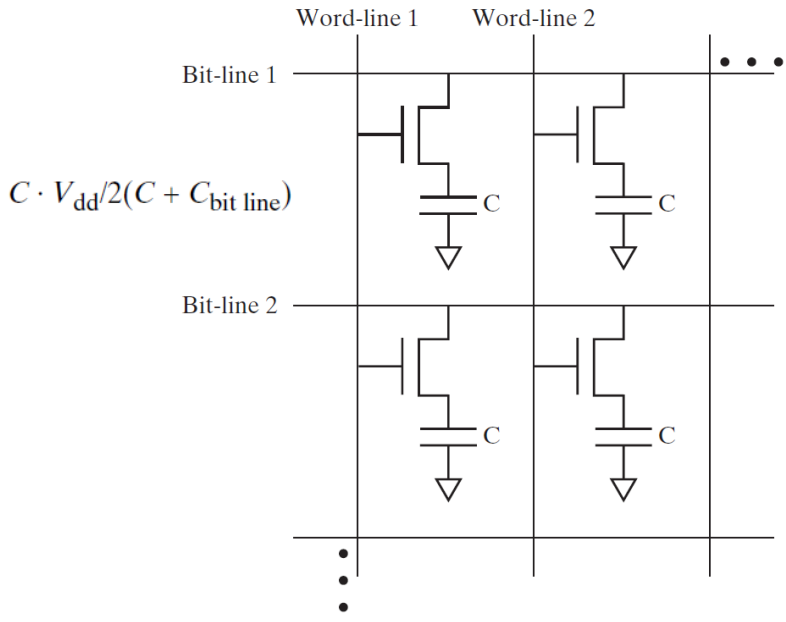




- One cell = 1 MOSFET + 1 Capacitor
- Needs to be refresh periodically

Source: *Prof. Yang-Kyu Choi, NT512*

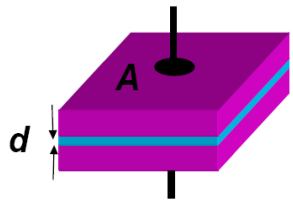
A schematic DRAM cell array



Slide 21

Evolution of DRAM Capacitor

Capacitance

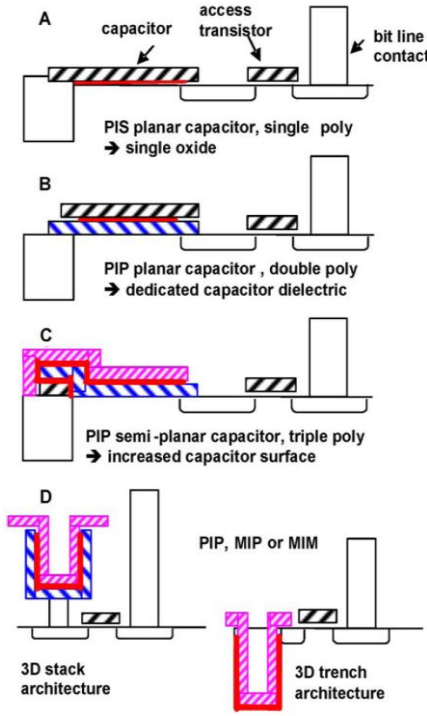


$$C = K\varepsilon_0 \frac{A}{d}$$

ε_0 = 8.85x10-14F/cm (Vacuum)
K= dielectric constant
d=dielectric thickness
A=area

- **To achieve large A, 3-D structure is highly demanded**
- **Thin dielectric (d ↓)**
  → leakage current ↑
- **High K dielectric :**
  - Ta_2O_5 : K= > 25
  - TiO_2 : K=30~40
  - ZrO_2 : K=14-28
  - Y_2O_3 : K=17
  - Si_3N_4 : K=7
  - BST (Ba, Sr)TiO_3 : K > 250

Source: *Prof. Yang-Kyu Choi, NT512*



Evolution of DRAM

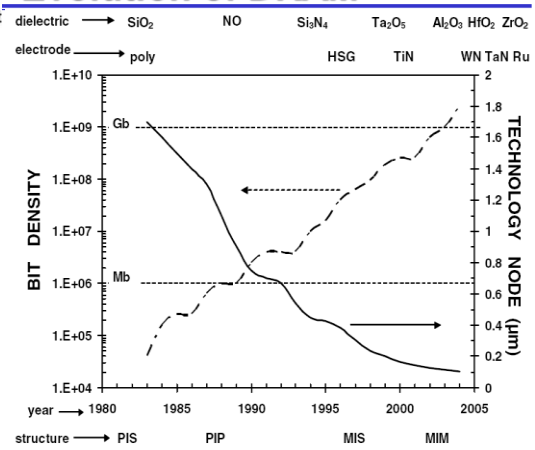
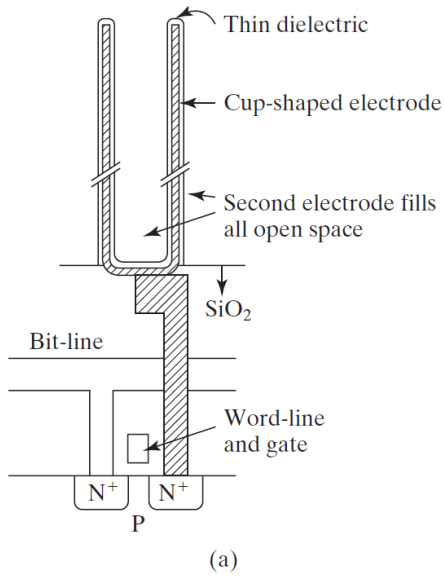


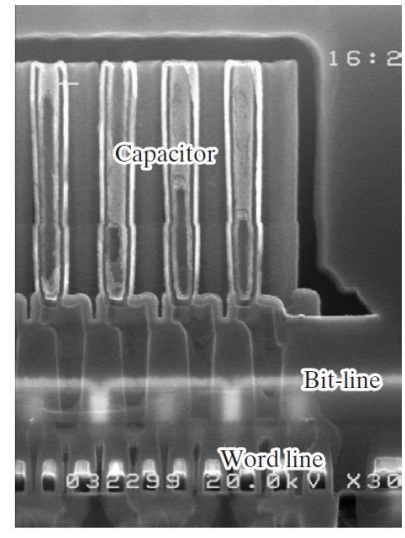
Fig. 3. Trend of DRAM production node, bit density, dielectrics and electrode materials.

Source: *Eric Gerritsen et al, SSE 49, (2005) 1767*

Fig. 1. DRAM architecture evolution from 1980 to 2005.



(a)



(b)

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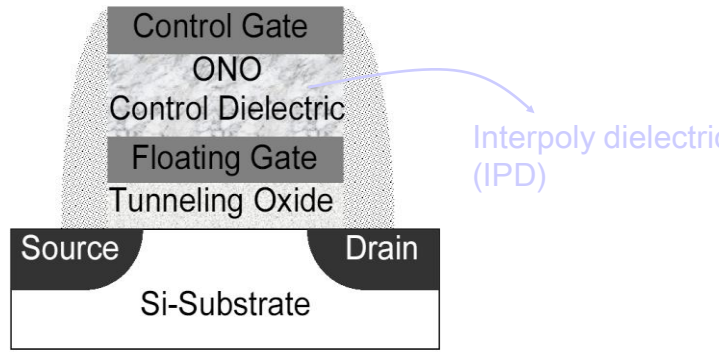
The Flash Cell

- Flash memory: A non-volatile, in-system-updateable, high-density memory technology that is per-bit programmable and per-block or per chip erasable
- In-system updateable: A memory whose contents can be easily modified by the system processor
- Block size: The number of cells that are erased at the same time



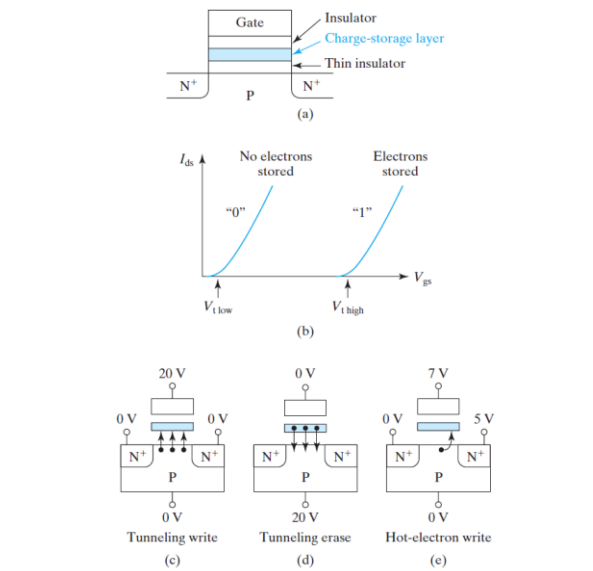
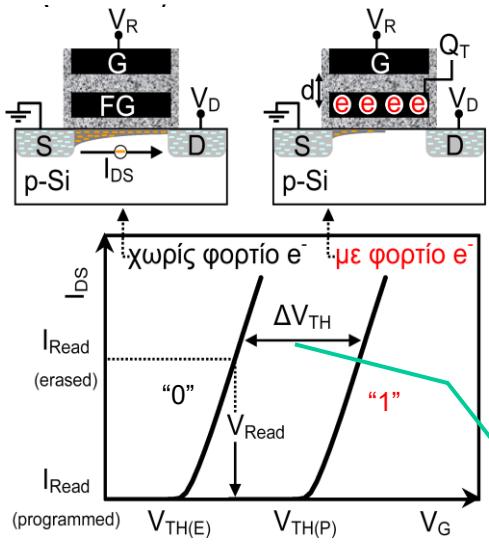


FIGURE 6–37 (a) A charge-storage NVM cell has a charge-storage layer in the gate dielectric stack; (b) V_t is modified by trapping electrons; (c) electron injection by tunneling; (d) electron removal by tunneling; and (e) electron injection by hot-electron injection.

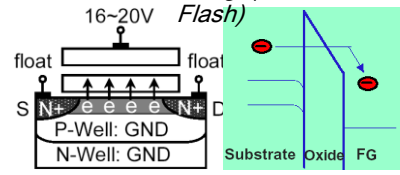
Το τρανζίστορ απομονωμένης πύλης (FG-MOSFET)

- Βασική αρχή

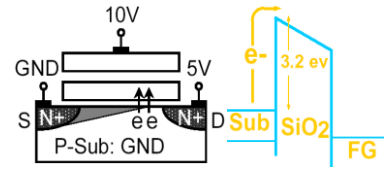


- Μηχανισμοί έγχυσης φορτίου

F-N Tunneling (NAND-Flash)



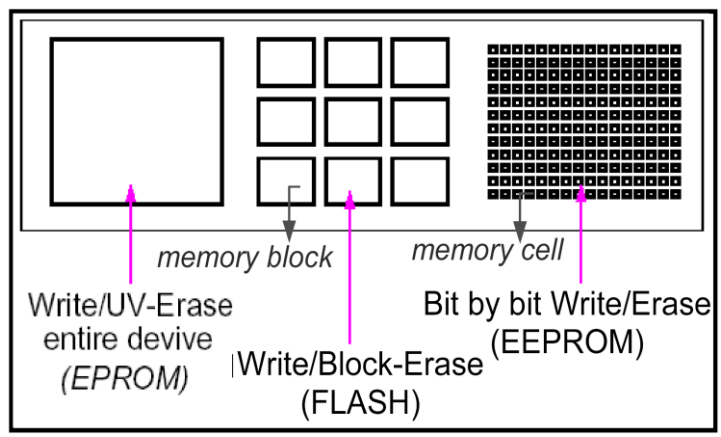
Hot Electron Injection (NOR-Flash)



Παράθυρο μνήμης:

$$\Delta V_{TH} = -\frac{Q_T}{\varepsilon_I} d$$

Απεικόνιση των εσωτερικών τμημάτων, που διαγράφονται ταυτόχρονα σε κάθε λειτουργία διαγραφής στους διάφορους τύπους της μνήμης NVM



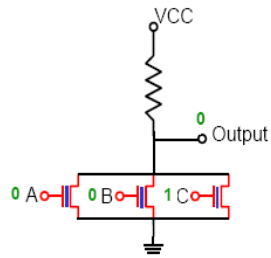
Boolean Logic

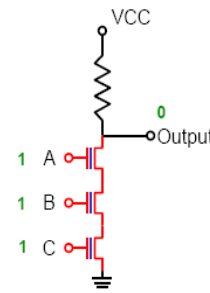
NOR

	A	B	C	Output
1	0	0	0	1
2	0	0	1	0
3	0	1	0	0
4	0	1	1	0
5	1	0	0	0
6	1	0	1	0
7	1	1	0	0
8	1	1	1	0

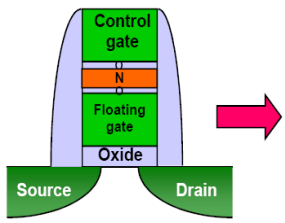
NAND

	A	B	C	Output
1	0	0	0	1
2	0	0	1	1
3	0	1	0	1
4	0	1	1	1
5	1	0	0	1
6	1	0	1	1
7	1	1	0	1
8	1	1	1	0

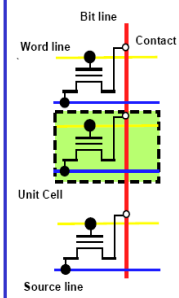
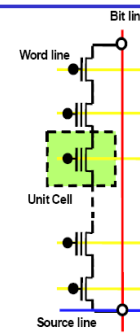
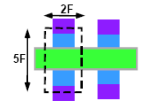
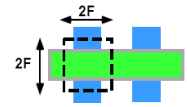
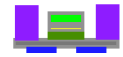
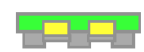




NOR and NAND

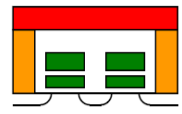
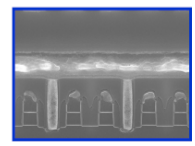
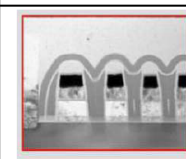


Single cell structure

	NOR	NAND
Cell Array		
Layout		
Cross section	 $10F^2$	 $4F^2$

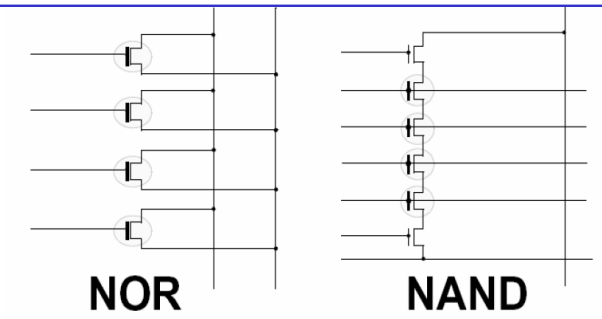
MXIC Macronix International Co., Ltd.

NOR and NAND Stacked Gate Flash

	NOR	NAND
		
Cell size (F^2)	10	5
Read access	Random (fast ~50ns)	Serial
Progr. Mechanism/ Troughput	CHE / 0.5 MB/s	FN / 7-10MB/s
SEM Cross-section (BL direction)		

Source: *L.Baldi, R.Bez – NanoE3 2008*

NAND vs. NOR



NOR

- Better E/W Endurance (>100K vs >10K)
- Random
- Fast Read (~100ns)
- Slow Write (~10 us)
- Used for Code

Not Scalable

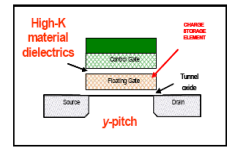
NAND

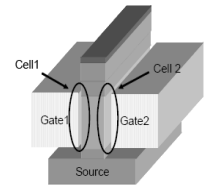
- Smaller Cell Size (~40%)
- Sequential
- Slow Read (~1 us)
- "Fast" Write (~1 us)
- Used for Data

Scalable

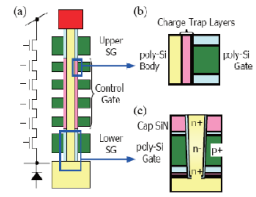
Innovations in Flash Technology

- **High-k dielectrics and "discrete-trap" memories**
  - Reduced oxide thickness
  - Lower energy barrier height
  - Improved reliability
- **Fin-FET and 3D architectures**
  - Vertical channel
  - Removes short channel problems
  - Limited by layer thickness of stacked gate
- **3D architectures**
  - Extend the scaling law, avoiding some critical process steps
  - Moves the scaling constraints along the vertical dimension.





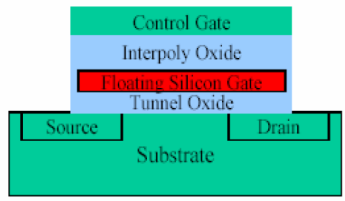
A. Fazio, MRS Bulletin, Nov. 2004



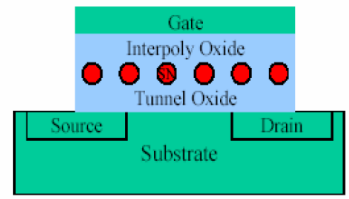
Source: *L.Baldi, R.Bez – NanoE3 2008*

Nanocrystal Storage

Floating Gate



Nanocrystal Storage



- Limits capacitive coupling between cells
- Reduces oxide defect induced charge leakage
- Thinner oxides permit lower programming voltage
- Reduced lateral charge flow – no drain turn-on
- Improves Scalability (70-20 nm per Samsung)
- Permits MLC storage

bprince@memorystrategies.com

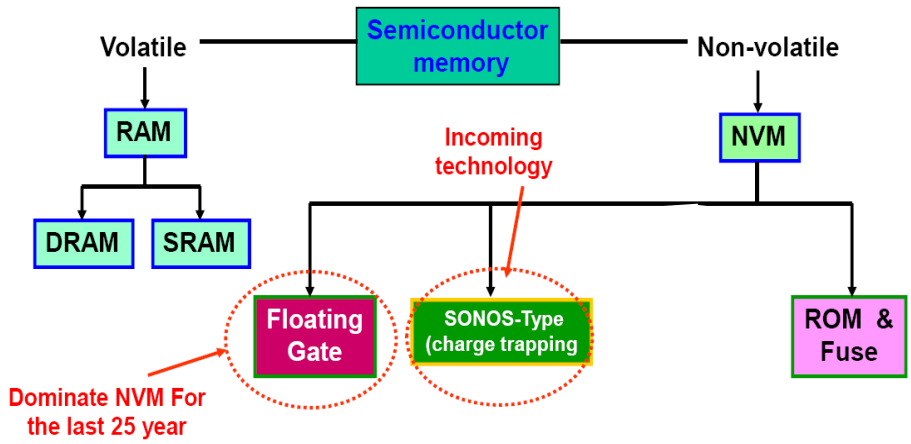
Mass storage: *Candidates for NAND*

Replacement: Charge trapping devices

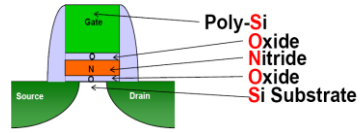
Those are not a floating gate device but a Nitride Charge trapping Device.

✓NROM (Saifun) is a NOR (with Virtual Ground array configuration)

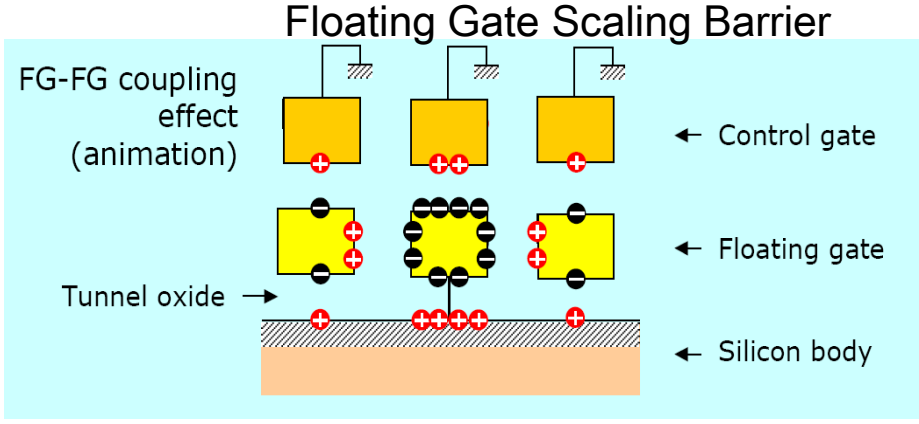
✓TANOS (Samsung) is a NAND SONOS



What is SONOS?



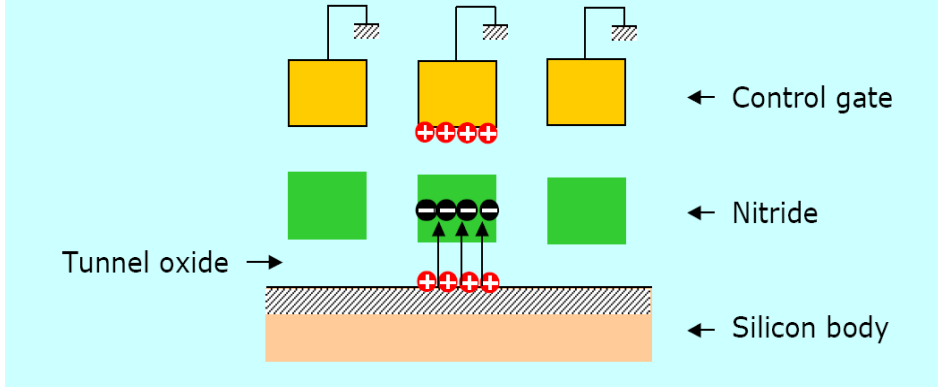
NAND Major Scaling Issue: Cell to Cell Proximity



- Floating gate electro-static interaction
  - Narrow floating-gate spacing
  - Tall floating gate

Nitride Storage

- The favorite NVM technology
  - Charge does not move around the storage electrode
  - Less floating gate electro-static interaction results in denser memories.



MultiLevel and Multi-bit

Multi-Level

Can do Multi-Level with FG/NC/SONOS

Multi-Bit

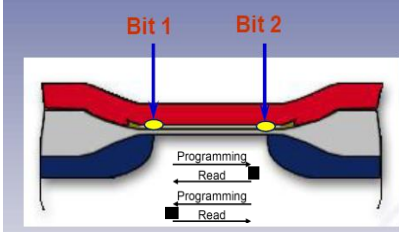
Move from Floating Gate to Nitride/Nanocrystal

Roadmap – 8 bit by 2010 (4-Multi-bit, 2 Multilevel?)

bprince@memorystrategies.com

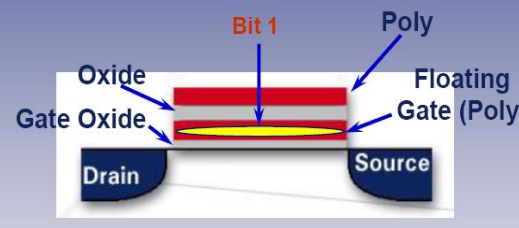
Multi-bit (NROM) vs. MultiLevel (Floating Gate)

NROM



- localized storage in nitride traps
- 2 *physical* bits per cell
- multi-level cell storage allows storage of 2 *electrical* bits per cell

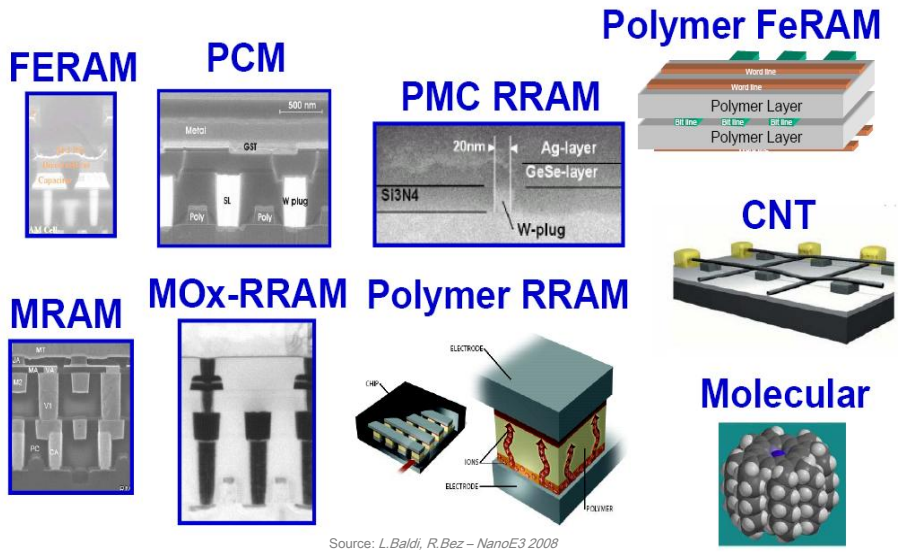
Floating Gate



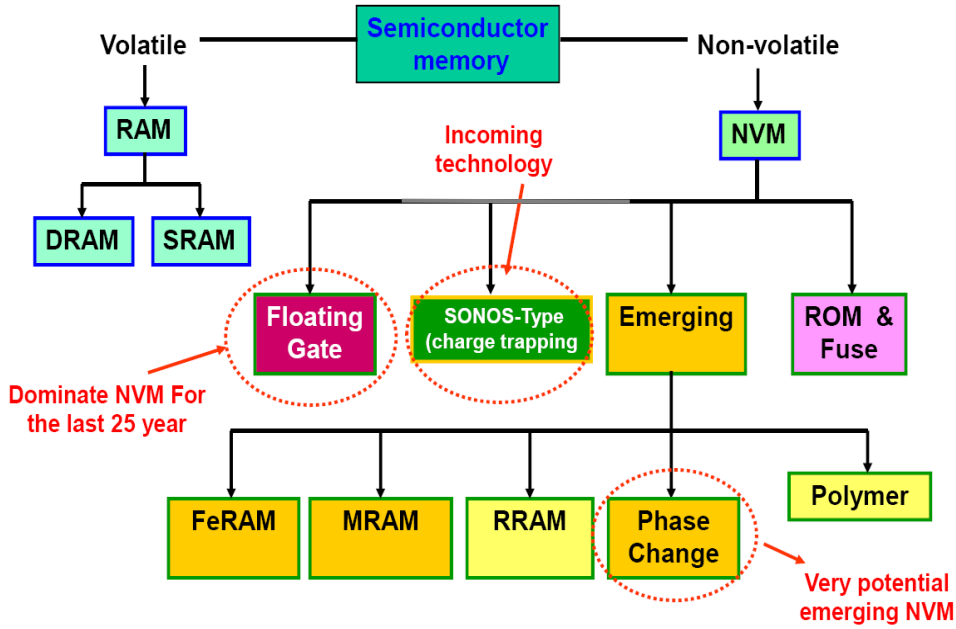
- physical storage of charge in floating gate
- multi-level cell storage allows storage of 2 or more *electrical* bits per cell

Near-Term and Long-Term Alternatives

More than 35 NVM alternatives have been so far proposed…



Source: *L.Baldi, R.Bez – NanoE3 2008*



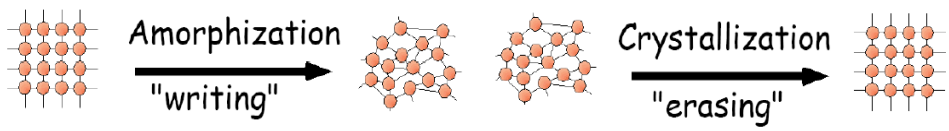
Near-Term and Long-Term Alternatives

Hysteretic Properties

- FeRAM (Ferroelectric RAM) → electric dipoles
- MRAM (Magnetic RAM) → resistance
- RRAM (Resistive RAM) → resistance
- Solid Electrolyte → resistance
- Phase Change Memory → resistance

Phase Change Materials

- **Same class of materials as the recording media of CD-RW and DVD-RW**
- **For DVD, a laser is used to write/erase by heating the GST**
  - High energy -> amorphous, low energy -> crystalline
  - Volume changes upon crystallization/amorphization changes the light scattered from the lower energy reading laser
- **For electrical phase change memory, the resistivity through the material is sensed by an external circuit**

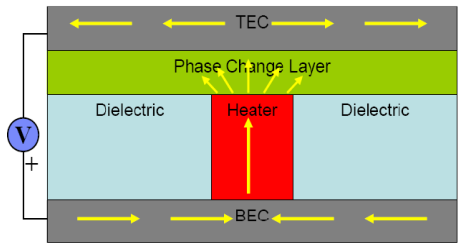


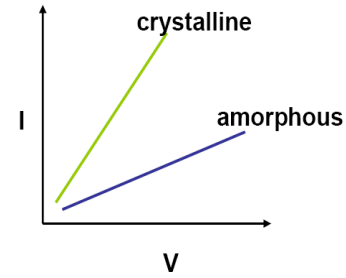
Source: H.-S. Philip Wong, Department of Electrical Engineering, Stanford University

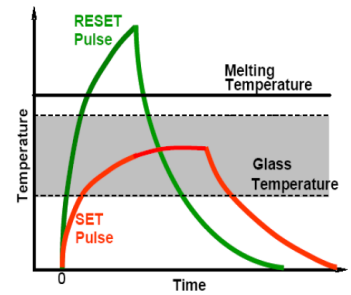
GeSbTe (**germanium-antimony-tellurium** or **GST**) is a *phase-change* material

Phase Change Memory

Operation Principle: Device operates by switching between *low resistance* SET state and *high resistance* RESET state.





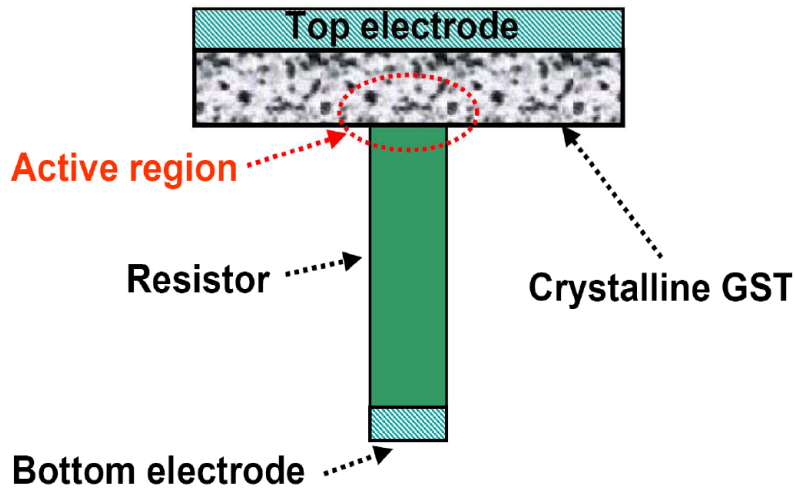


Electrical current pulses lead to intense localized heating (~10^{11}K/s) in the phase change layer.

Controlled pulses cause transition between the high resistivity amorphous phase and low resistivity crystalline phase.

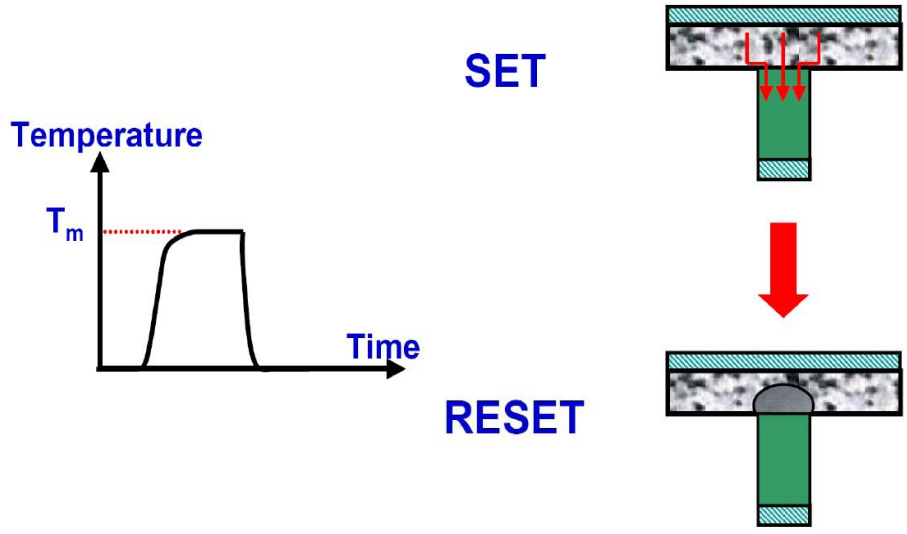
Source: H.-S. Philip Wong, Department of Electrical Engineering, Stanford University

Typical Phase Change Memory Device Structure



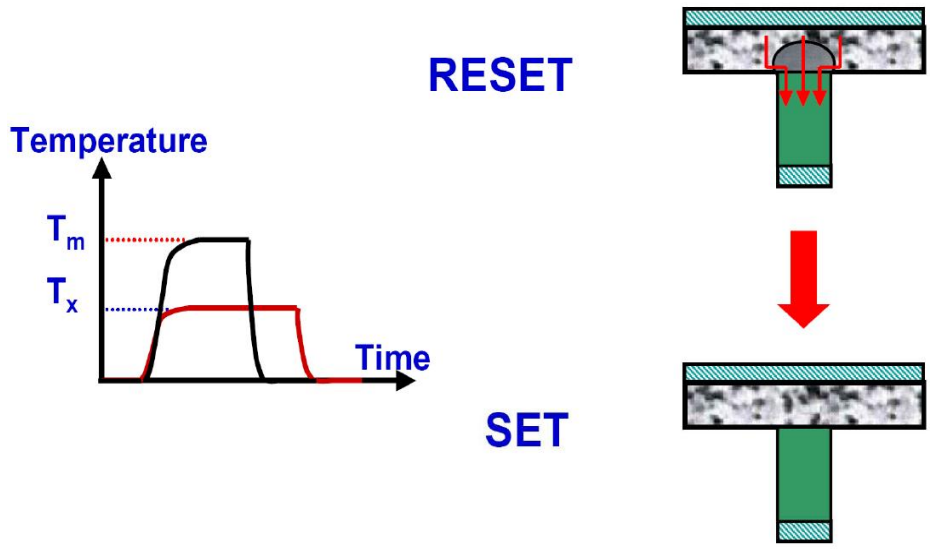
A. Pirovano, "Emerging Non-Volatile Memories," *IEDM Short Course* ,2006.

PCM – SET to RESET



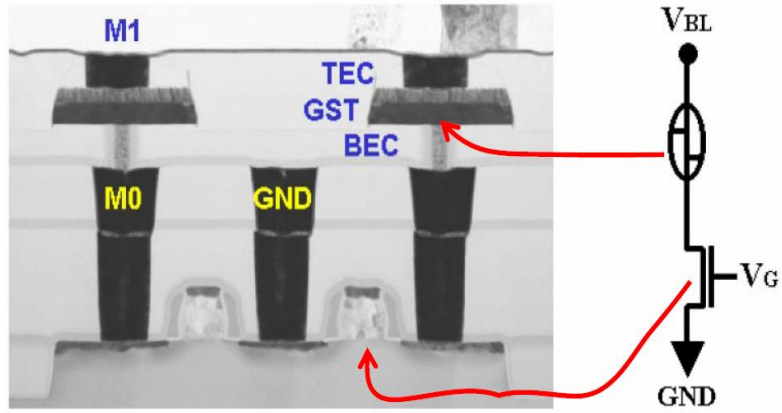
A. Pirovano, "Emerging Non-Volatile Memories," *IEDM Short Course* ,2006.

PCM – RESET to SET



A. Pirovano, "Emerging Non-Volatile Memories," *IEDM Short Course* ,2006.

Experimental Phase Change Memory Cells

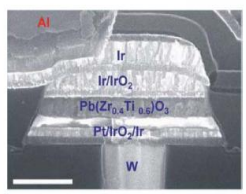


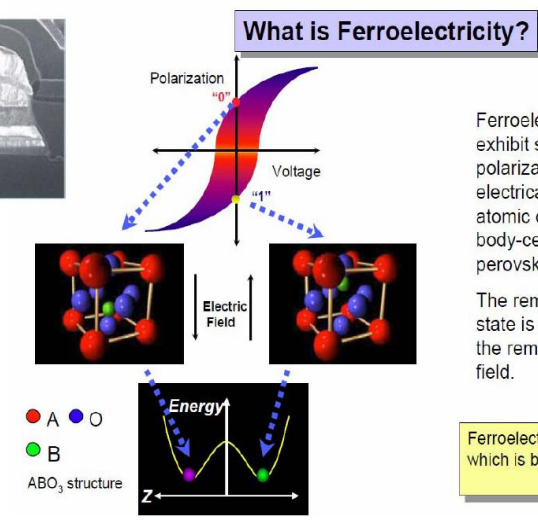
Y. N. Hwang, S. H. Lee, S. J. Ahn, S. Y. Lee, K. C. Ryoo, H. S. Hong, H. C. Koo, F. Yeung, J. H. Oh, H. J. Kim, W. C. Jeong, J. H. Park, H. Horii, Y. H. Ha, J. H. Yi, G. H. Koh, G. T. Jeong, H. S. Jeong, and K. Kim, "Writing current reduction for high-density phase-change RAM," *IEDM Tech. Dig.*, pp. 893 - 896, December 2003.

FeRAM (Ferroelectric RAM)

- Ferroelectric **RAM**
- Remanent polarization of ferroelectric materials

Source: Samsung





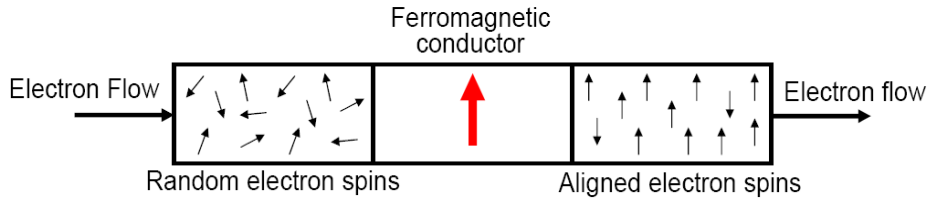
Ferroelectric materials exhibit spontaneous polarization with applied electrical field due to the atomic displacement of the body-centered atom in the perovskite(ABO_3) structure.

The remnant polarization state is maintained after the removal of the electric field.

Ferroelectric has "**two**" stable states, which is basis of memory application

MRAM (Magnetic RAM): *Spin-Polarized Current*

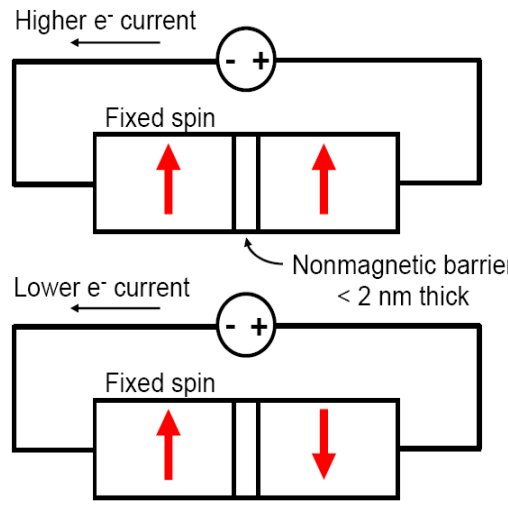
- The spin of the electrons making up the current in most electronic devices is irrelevant to circuit operation.
- However, spin is a property that can potentially be controlled and exploited to make useful new devices
  ⇒ an emerging field called "spintronics"
- The spin of the moving electrons tends to line up with an environment of aligned spin, like the magnetic field present in a piece of polarized ferromagnetic material.



Source: Bruce F. Cockburn, 2006 Emerging Technologies Workshop

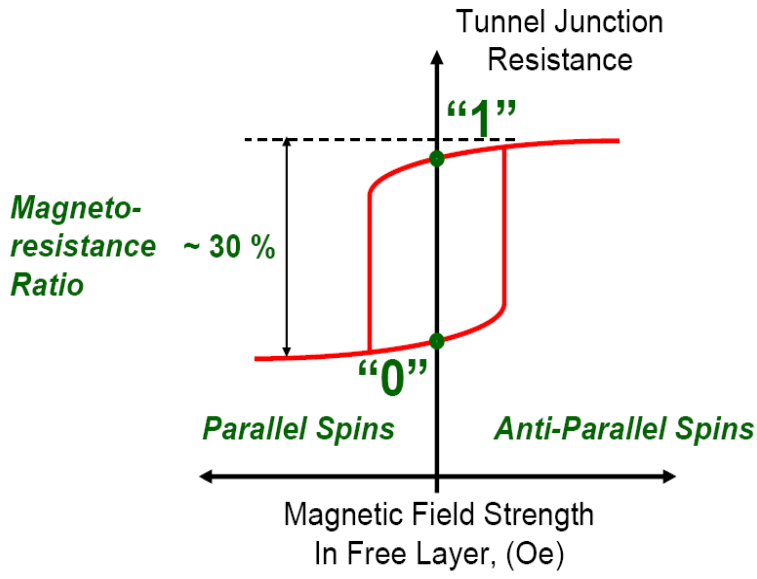
The Magnetic Tunnel Junction

1) Parallel Spins
   - lower barrier to tunneling current
   - > 30% resistance drop
   - higher current
2) Anti-parallel Spins
   - higher barrier to tunneling current
   - lower current



Source: Bruce F. Cockburn, 2006 Emerging Technologies Workshop

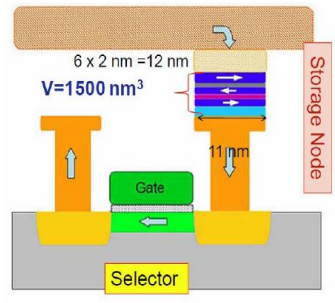
MRAM Cell Hysteresis



Source: Bruce F. Cockburn, 2006 Emerging Technologies Workshop

MRAM (Magnetic RAM)

- MRAM is a new generation of much faster magnetic memory that is compatible with semiconductor integrated circuit technology.



Source: R.Cavin & V. Zhirnov, SRC

• Understanding MTJ MRAM operation requires understanding of some basic properties of spin-polarized current.

Main Alternative NVM Concepts

	FRAM (ferroelectric)	MRAM (magnetic)	PCM (phase change)
Storage Mechanism	Permanent polarization of a ferroelectric material (PZT or SBT)	Permanent magnetization of a ferromagnetic material in a MTJ	Amorphous/poly-crystal phases of chalcogenide alloy
Cell Size F^2 (ITRS)	Large: 22→16	Large: 22→17	Small: 5→4 (BJT) Medium: 15→7.4 (Tx)
Scalability	Poor	Poor	Good
Endurance	10^{10} (destructive read)	$>10^{14}$	10^{12}
Write	Low power capacitive Theoretically good speed	Power constrained, Scales poorly	Power constrained, Improves with scaling
Application	Embedded, Low Density	Embedded, Low Density	Stand Alone or Embedded High Density, Low Cost
Maturity	Limited prod.	Test chips	Prototypes

Source: *L.Baldi, R.Bez – NanoE3 2008*

Cell architectures for RAM cells

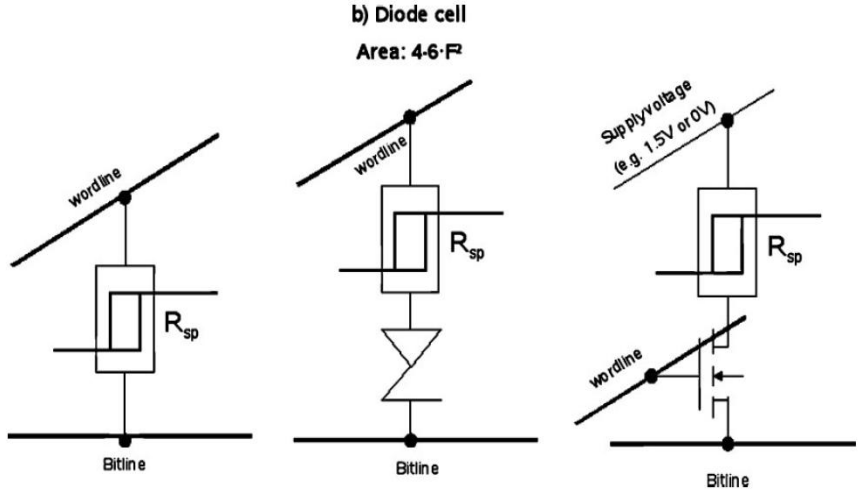
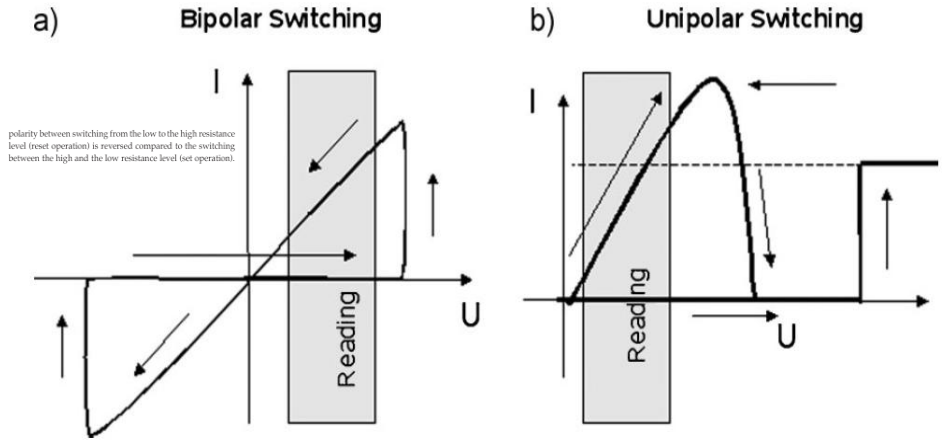


Fig. 2. Three different cell architectures for resistive memory cells: (a) cross-point cell, (b) diode cell, and (c) transistor cell together with their respective area consumption in F^2. F denotes the minimum feature size of the fabrication technology.

Thomas Mikolajick et al, ADVANCED ENGINEERING MATERIALS 2009, 11, 235-240

Typical current–voltage characteristics for (a) bipolar and (b) unipolar switching



polarity between switching from the low to the high resistance level (reset operation) is reversed compared to the switching between the high and the low resistance level (set operation).

Fig. 3. Typical current–voltage characteristics for (a) bipolar and (b) unipolar switching.

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RRAM Proposed Alternatives

Chalcogenide

- GST and other phase-change alloys
- AgGeSe, AgGeS, WO_3 and SiO_2 solid electrolyte

Binary oxide

- Nb_2O_5, Al_2O_3, Ta_2O_5, TiO_2, ZrO_x , Cu_xO and NiO

Oxides with perovskite structure

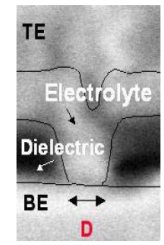
- $SrZrO_3$, doped- $SrTiO_3$, $Pb(Zr_xTi_{1-x})O_3$ and $Pr_{0.7}Ca_{0.3}MnO_3$

Conductive polymers

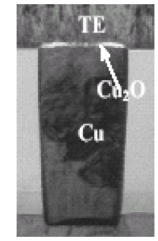
- Bengala Rose, AlQ_3Ag, Cu-TCNQ

In common:

Storage mechanism(s) still debated



M. Kozicki, EPCOS 2006



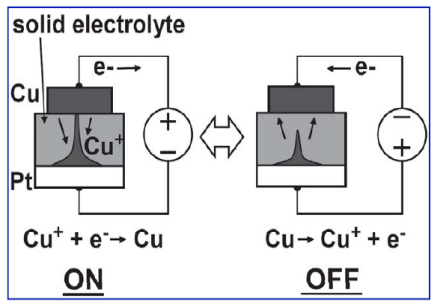
A. Chen *et al.*,
IEDM Tech. Dig. 2005

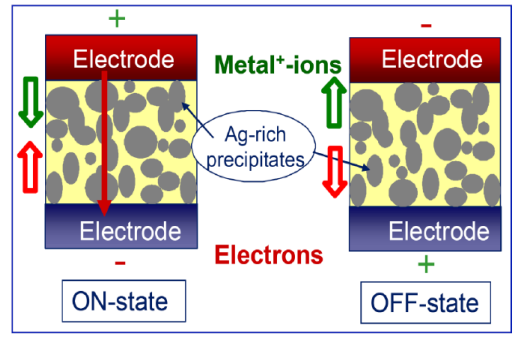
Source: *L.Baldi, R.Bez – NanoE3 2008*

Solid Electolyte

1. Redox reaction
2. Ion migration (cation toward cathode)

$M \rightarrow M^+ + e^-$
$M \leftarrow M^+ + e^-$





Cu/Cu_2S **Ag-Ge-Se**

M. Kund et al., "Conductive bridging RAM (CBRAM): an emerging non-volatile memory technology scalable to sub 20 nm," IEDM, p. 754 (2005).
T. Sakamoto et al., "A Ta_2O_5 solid-electrolyte switch with improved reliability," Symp. VLSI Technology, p. 38 (2007).

Candidate NVM Alternatives

- **Improved Flash**…….. limited scalability/endurance
- **FeRAM (Ferroelectric RAM)**……limited scalability
- **MRAM (Magnetic RAM)**…….. write current too high
- **RRAM (Resistive RAM)**……significant problems to resolve
- **Solid Electrolyte**…….. in development, promising
- **Phase Change Memory**…. it's going to happen