

ML505/506/507 BSB Design
Adding Standard IP

May 2010

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ML505 Standard IP Design Overview

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  - Using the Pre-Built Design
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  - Generate the Bitstream
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- **Create an ACE File**
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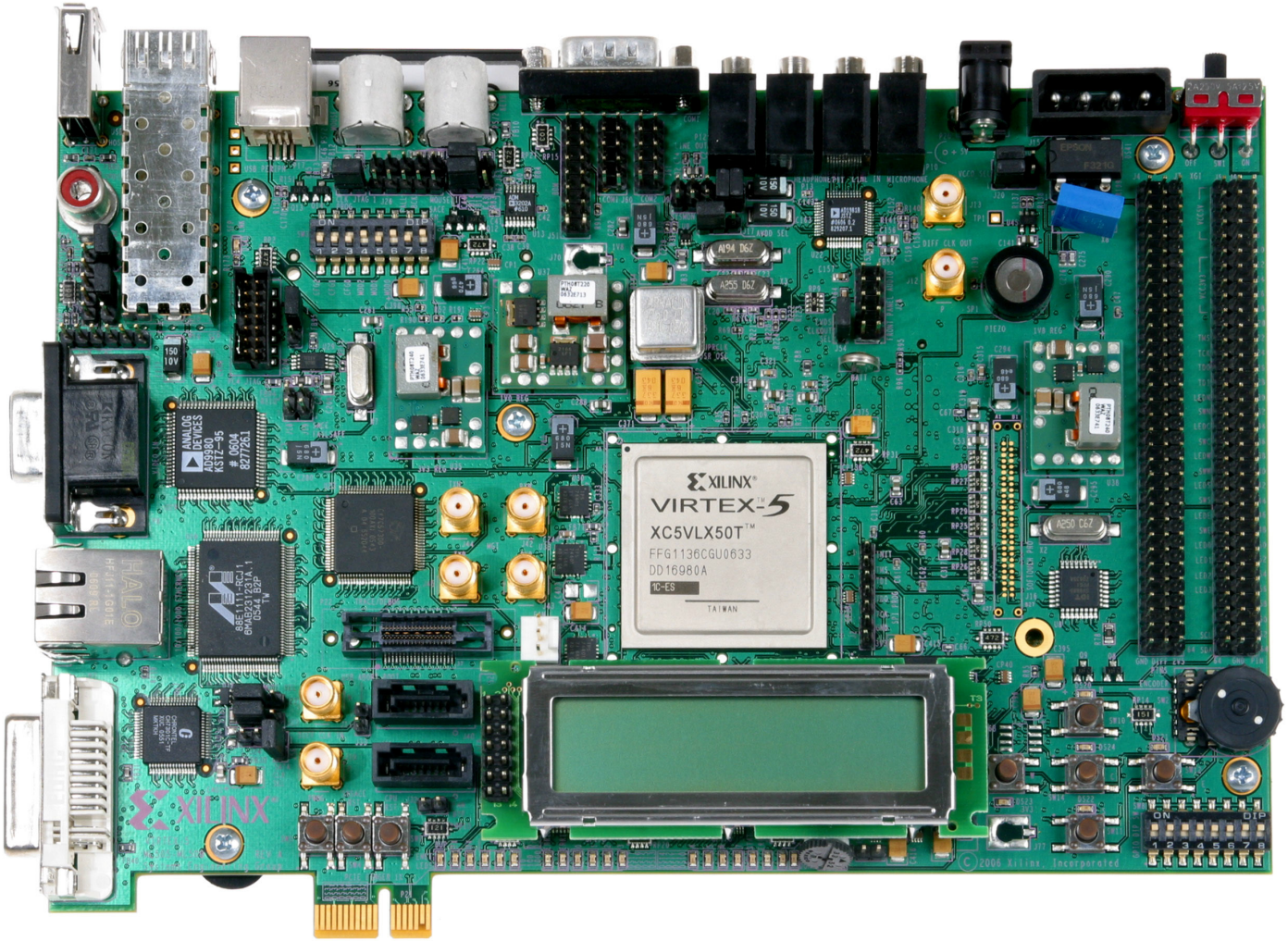
Note: This Presentation applies to the ML505, ML506, and ML507

ML505 Standard IP Design Overview

- **Standard IP Added:**
  - TFT – xps_tft
  - PS/2 – xps_ps2
  - General Purpose IO – xps_gpio
  - IIC Interface – xps_iic
- **Standard IP Modified:**
  - SRAM Interface – xps_mch_emc

Note: Presentation applies to the ML505, ML506, and ML507

Xilinx ML505 Board

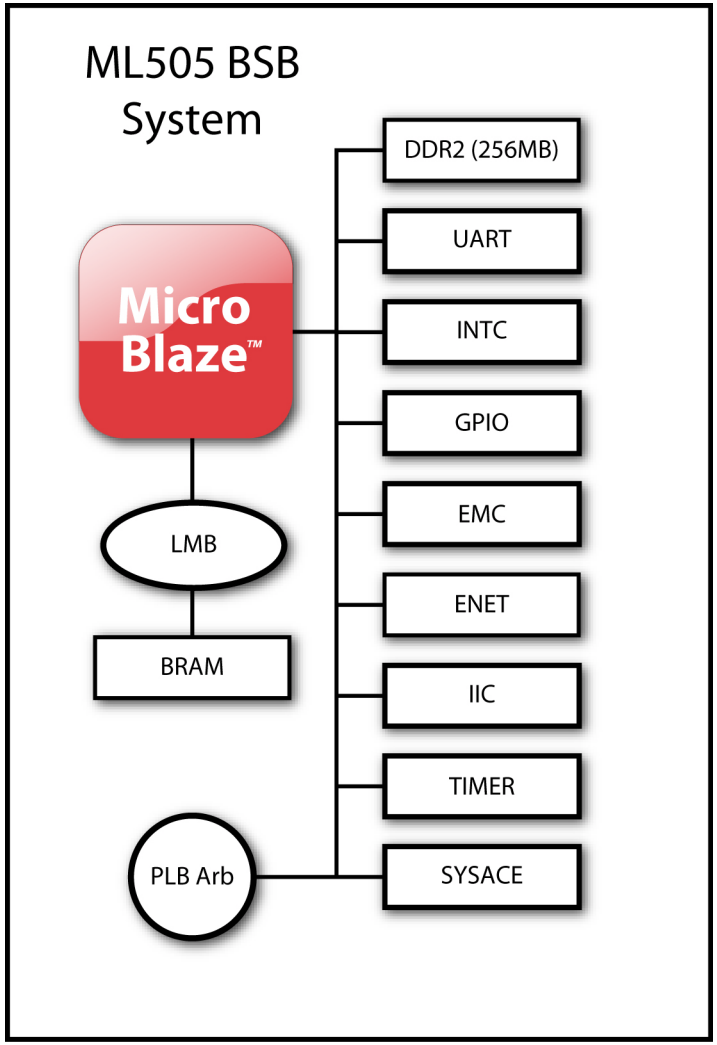


Note: Presentation applies to the ML505, ML506, and ML507

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ML505 Base System Builder Hardware

- **The ML505 MicroBlaze BSB Design Hardware includes:**
  - DDR2 Interface (256 MB)
  - BRAM
  - External Memory Controller (EMC)
  - ZBT SRAM
  - Networking
  - UART
  - Interrupt Controller
  - System ACE CF Interface
  - GPIO (IIC, LEDs and LCD)
  - PLB Arbiter



Note: Presentation applies to the ML505, ML506, and ML507

ISE Software Requirements

- **Xilinx ISE 12.1 software**



Note: Presentation applies to the ML505, ML506, and ML507

EDK Software Requirement

- **Xilinx EDK 12.1 software**



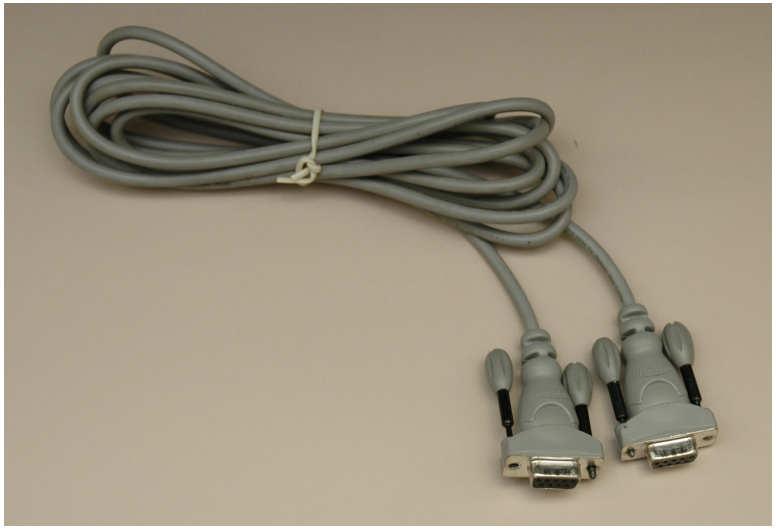
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ML505 Setup

- Connect the Xilinx Platform Cable USB to the ML505 board



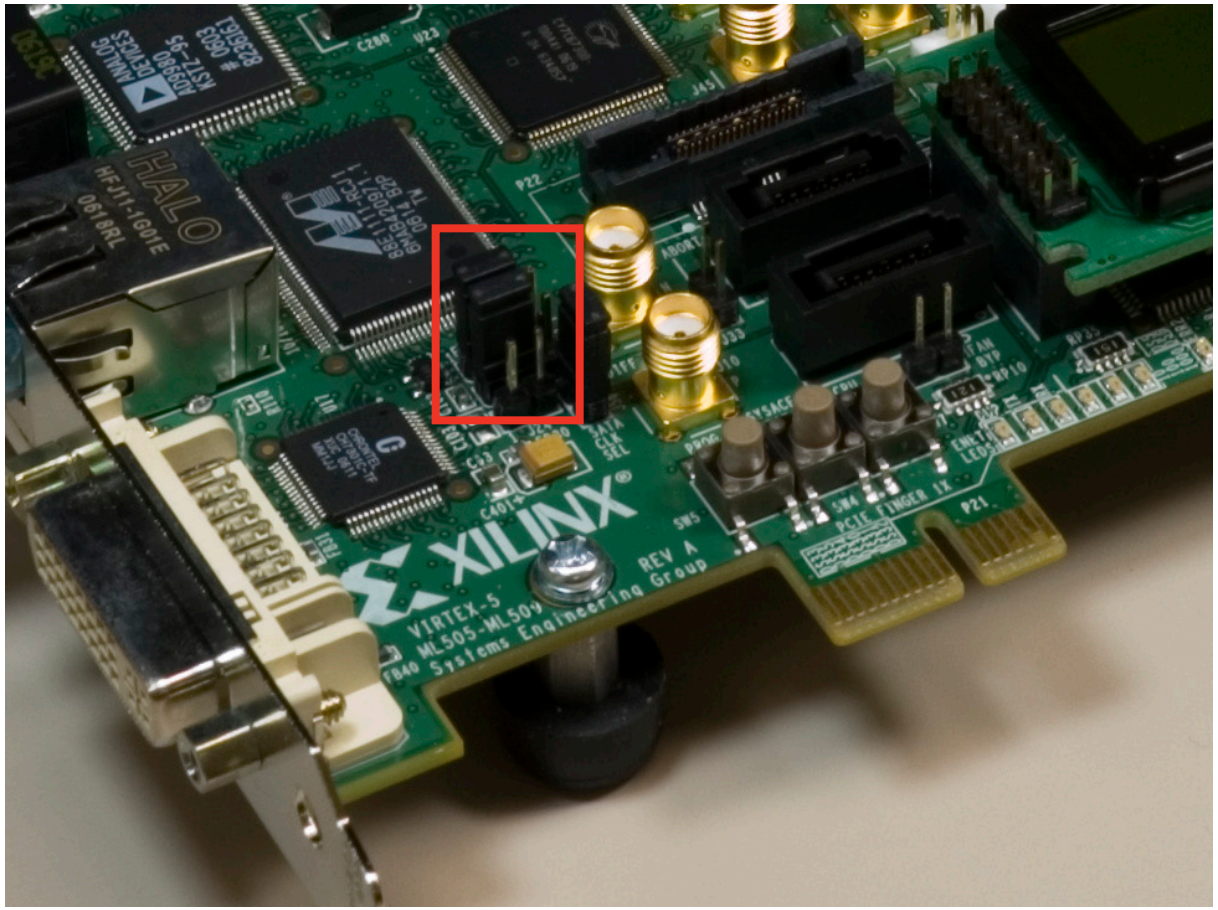
- Connect the RS232 null modem cable to the ML505 board



Note: Presentation applies to the ML505, ML506, and ML507

ML505 Setup

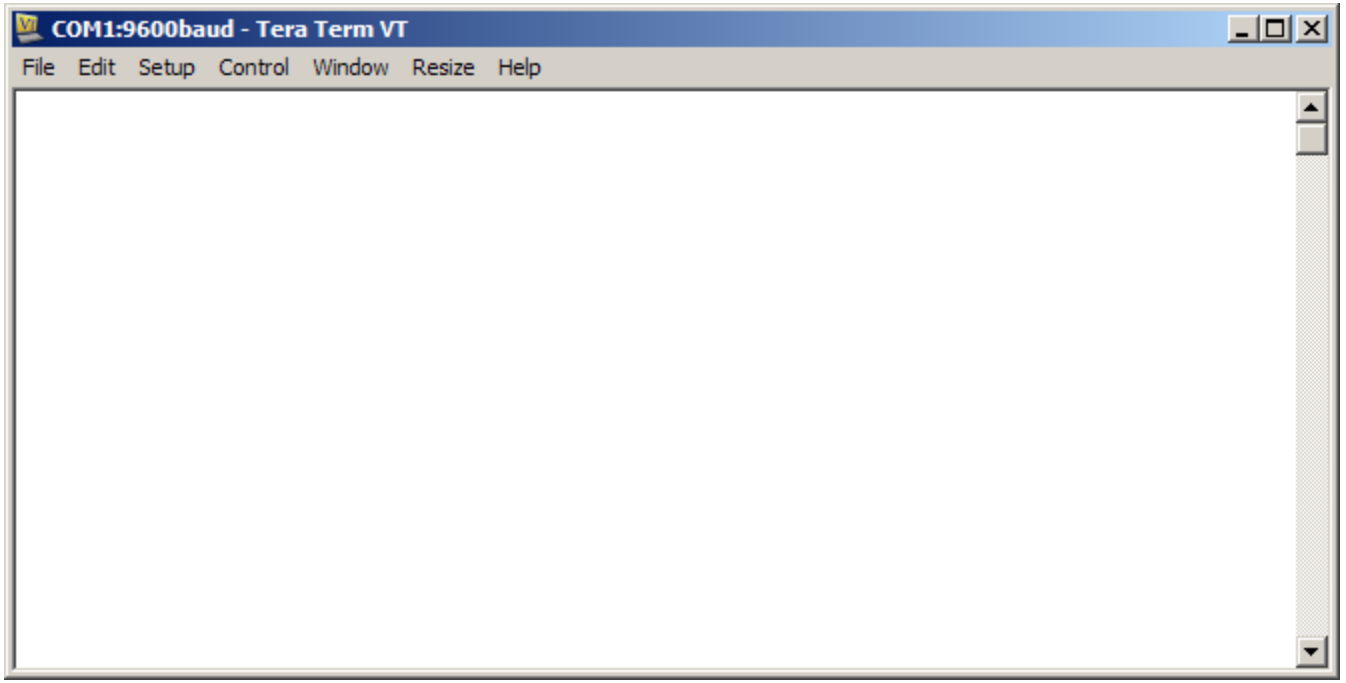
- **Set ML505 Jumpers for GMII**
  - Set both J22 and J23 to positions 1-2 (as shown)



Note: Presentation applies to the ML505, ML506, and ML507

ML505 Setup

- **Start the Terminal Program:**



Note: Presentation applies to the ML505, ML506, and ML507

Additional ML505 Setup Details

- **Refer to ml505_overview_setup.ppt for details on:**
  - Software Requirements
  - ML505/506/507 Board Setup
  - Equipment and Cables
  - Software
  - Network
- **Terminal Programs**
  - This presentation requires the 9600-8-N-1 Baud terminal setup



Note: Presentation applies to the ML505, ML506, and ML507

Using the Pre-Built Design

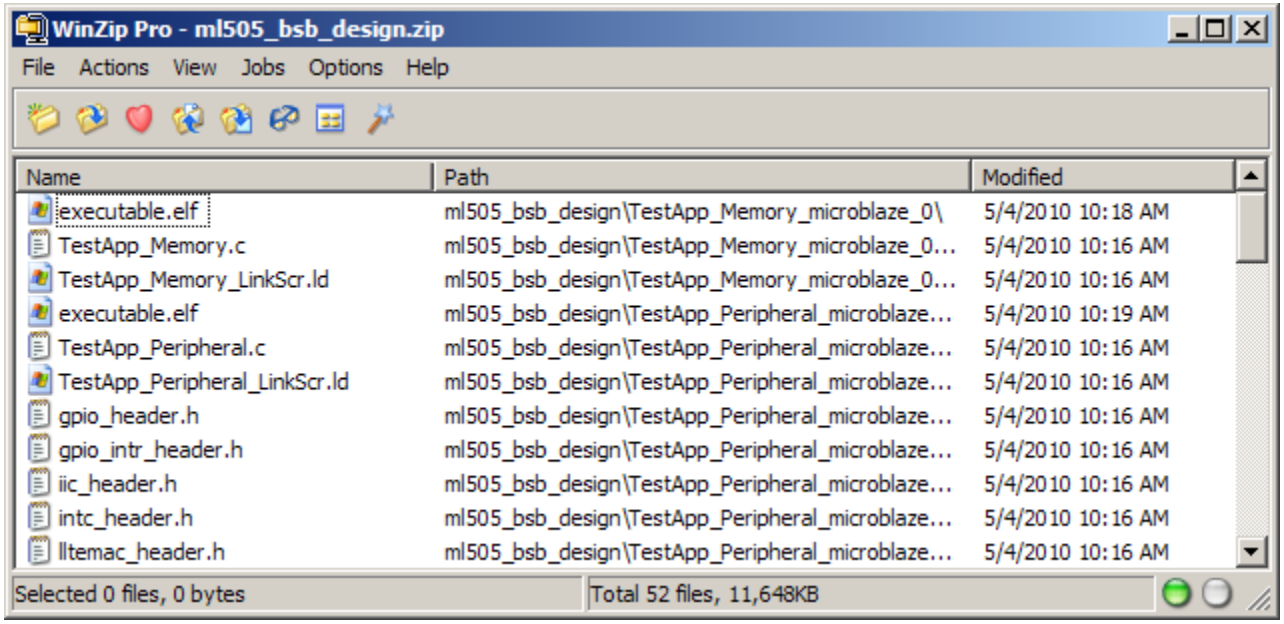
- **Unzip ml505_bsb_std_ip.zip and locate pre-built bitstream and executable software files:**
  - ml505_bsb_std_ip/implementation/download.bit
  - ml505_bsb_std_ip/microblaze_0/code/*.elf
- **Configure FPGA**
  - Launch XPS project, ml505_bsb_system.xmp
  - From the menu, select Project → Launch EDK Shell and type:

    impact -batch etc/download.cmd
  - Go to Slide 92, to run the software application
- **For a tutorial on how to create the contents of the ml505_bsb_std_ip.zip continue to the next slide**

Add Standard IP to BSB Design

Extracting the Design

- **Unzip the ml505_bsb_design.zip file**
  - This creates ISE and EDK project directories

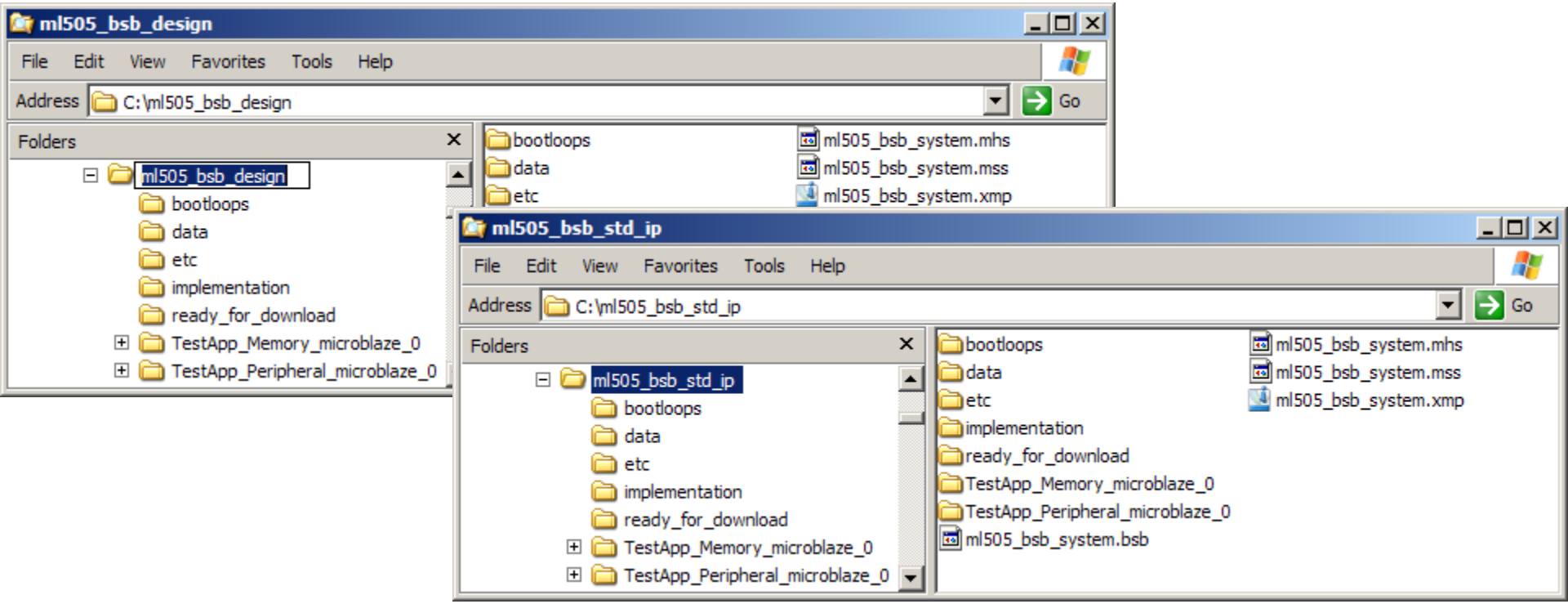


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Extracting the Design

- **Rename the project directory to**

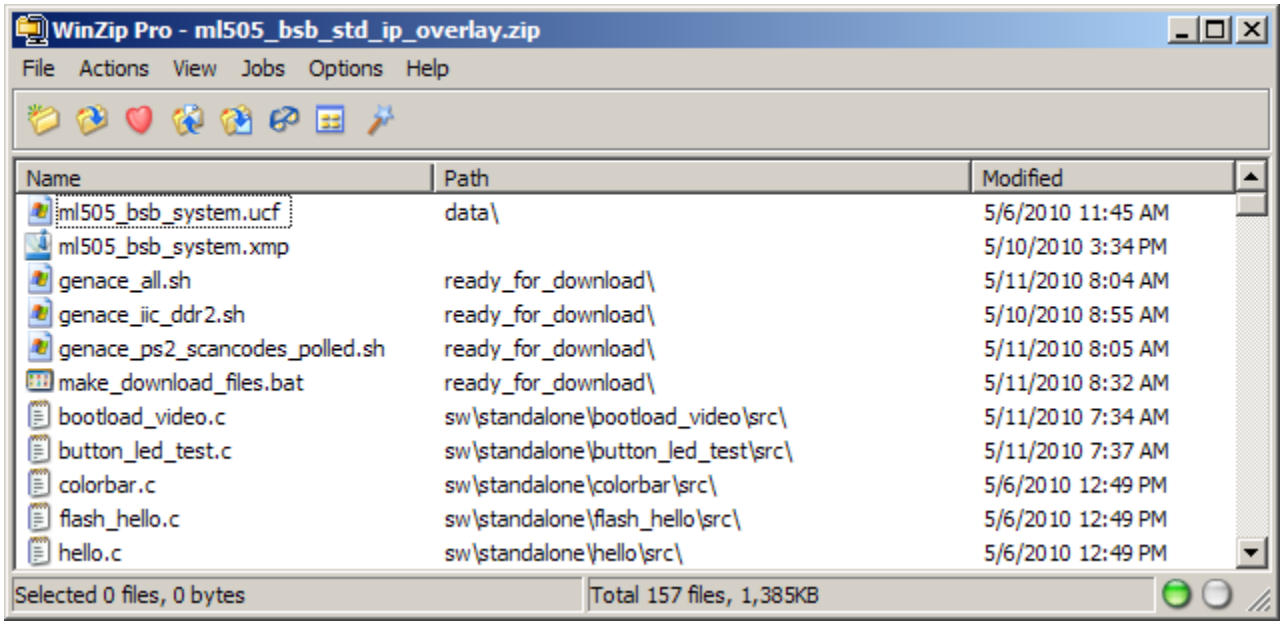
  ml505_bsb_std_ip



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Extracting the Design

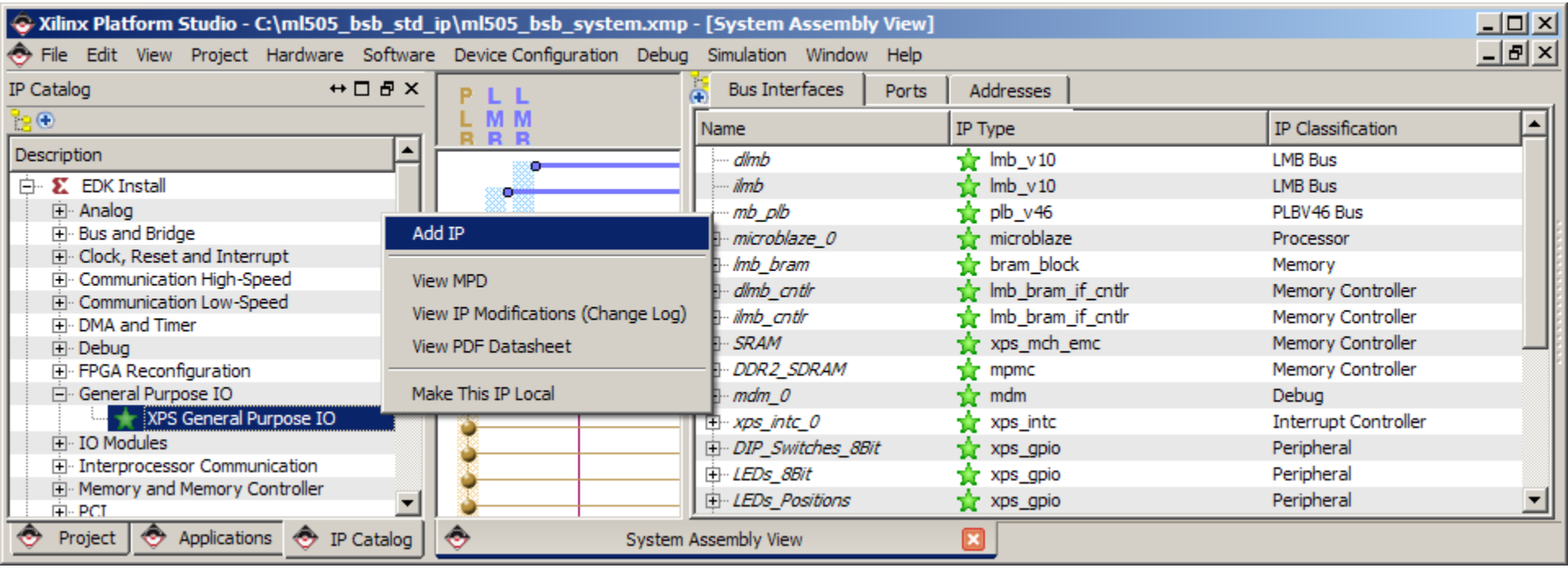
- **Unzip the ml505_bsb_std_ip_overlay.zip file**
  - Unzip to the ml505_bsb_std_ip directory
  - This adds the Standard IP UCF and software to the design directory
  - For ML506 use ml506_bsb_std_ip_overlay.zip
  - For ML507 use ml507_bsb_std_ip_overlay.zip



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Add Standard IP

- Open XPS project <design path>\ml505_bsb_system.xmp
- Add General Purpose IO
  - Right-click on the **XPS General Purpose IO**
  - Select **Add IP …**

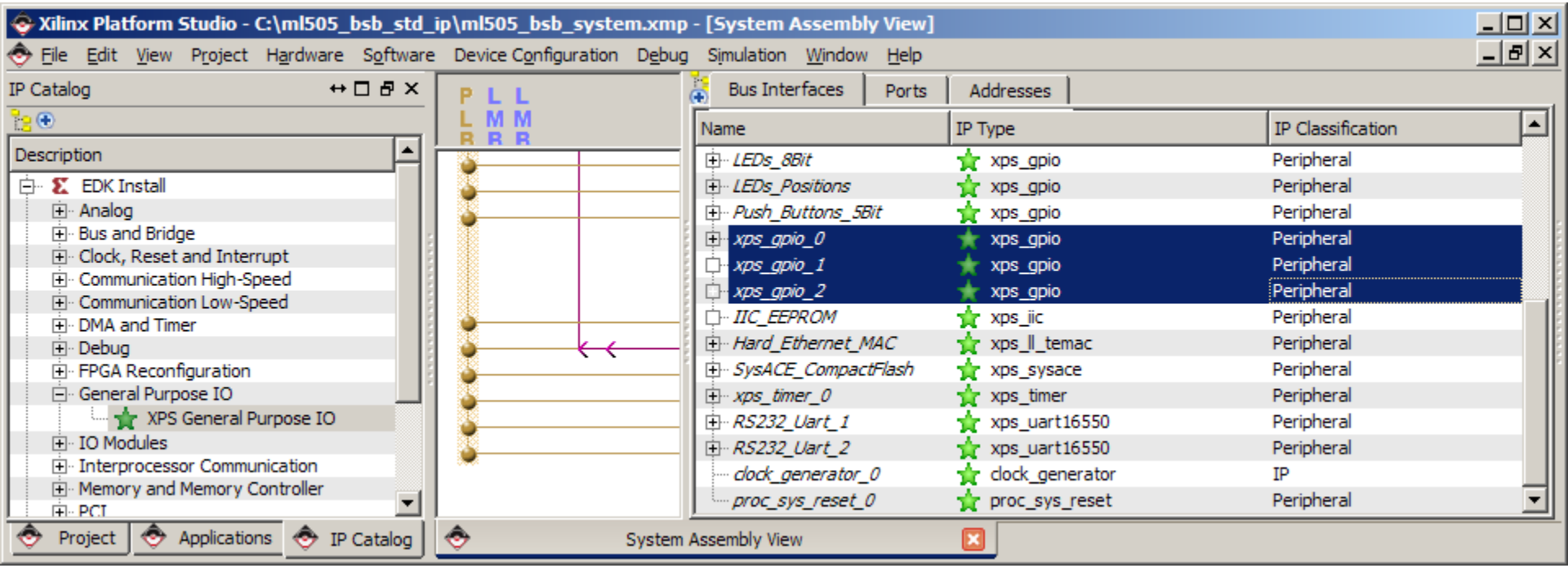


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Add Standard IP

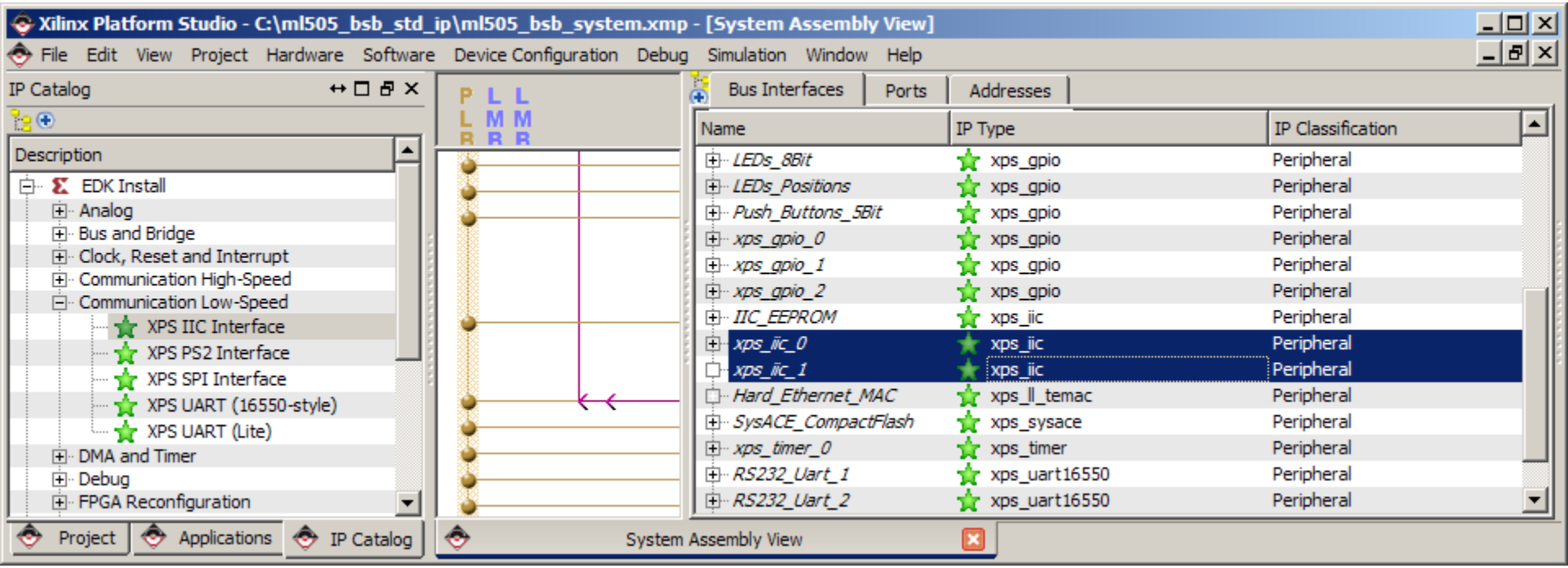
- **Add General Purpose IO**
  - Add 2 more instances of the XPS General Purpose IO IP



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Add Standard IP

- **Add two instances of the XPS IIC Interface**
  - Right-click on XPS IIC Interface
  - Select **Add IP…**
  - Repeat for second instance

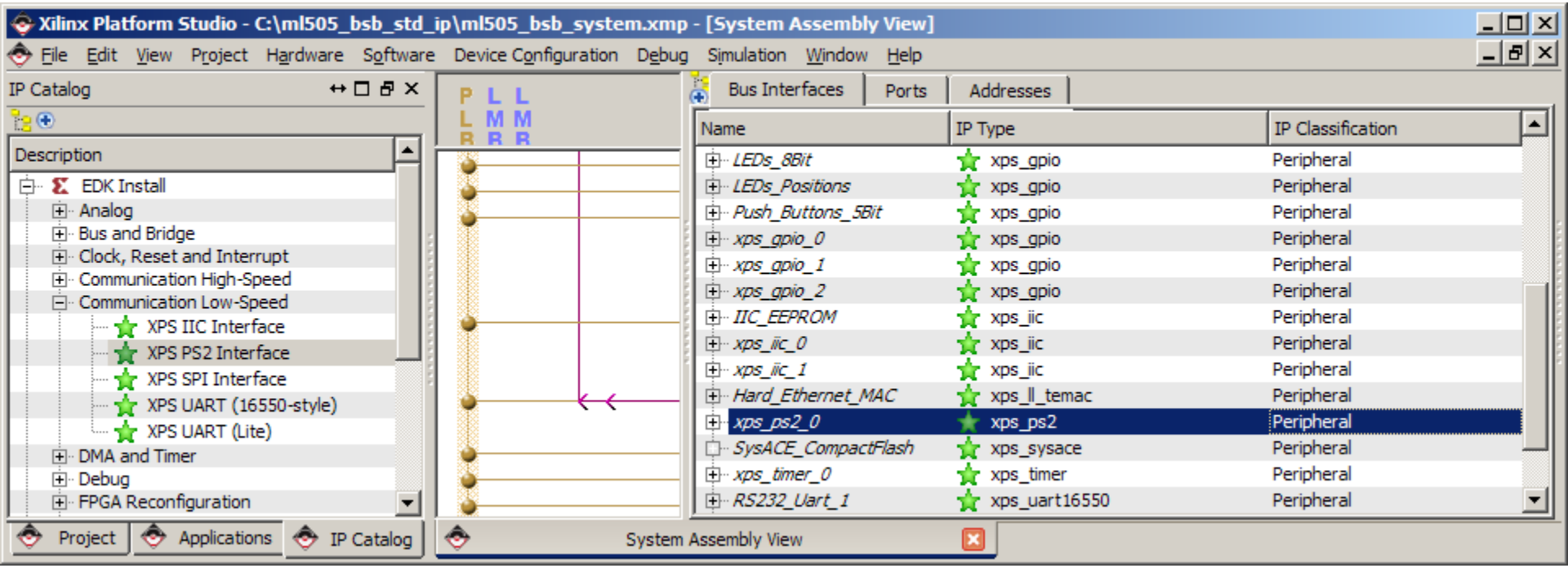


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Add Standard IP

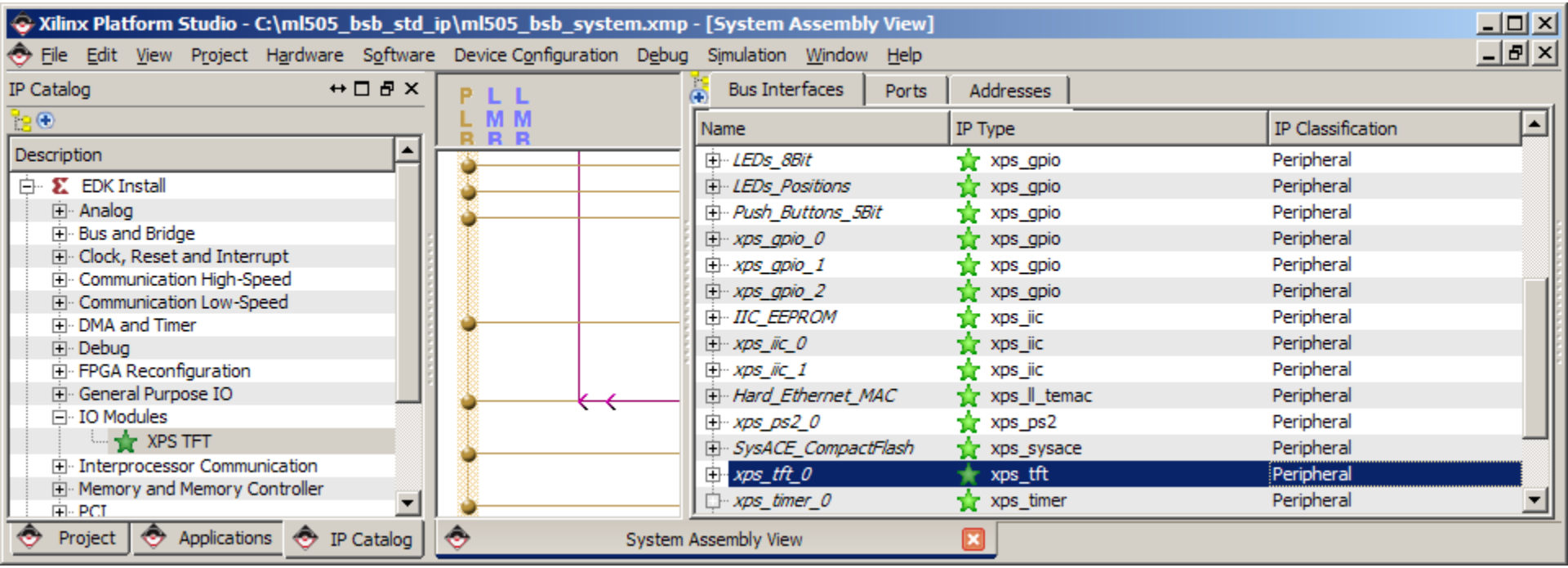
- **Add PS/2 Interface**
  - Right-click on **XPS PS2 Interface**
  - Select **Add IP…**



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Add Standard IP

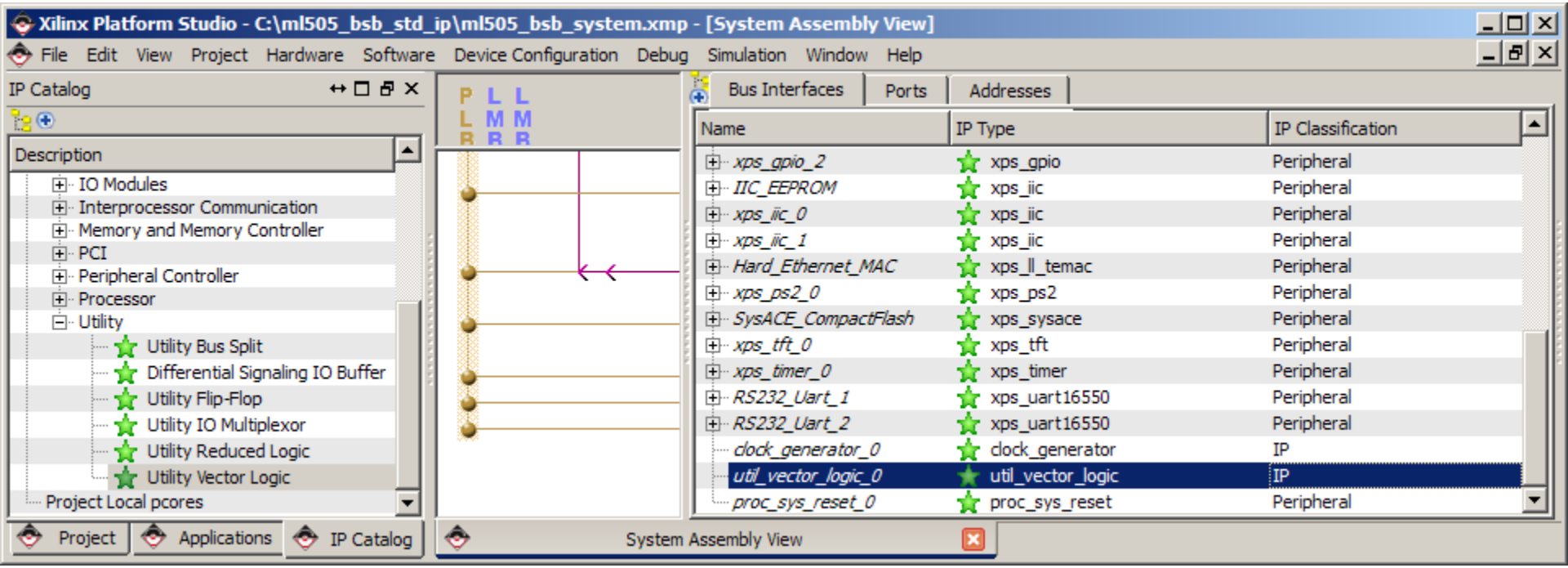
- **Add Video Controller**
  - Right-click on **XPS TFT**
  - Select **Add IP…**



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Add Standard IP

- **Add an Inverter**
  - Right-click on **Utility Vector Logic**
  - Select **Add IP…**

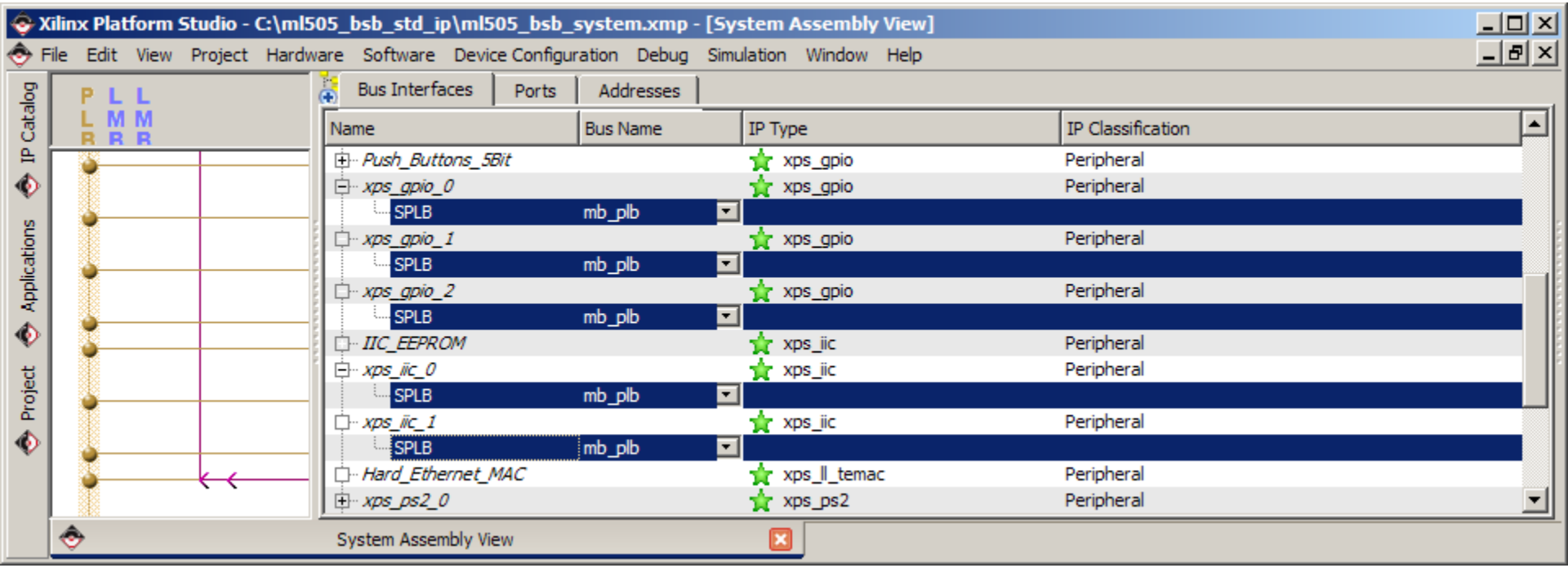


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Connect Buses

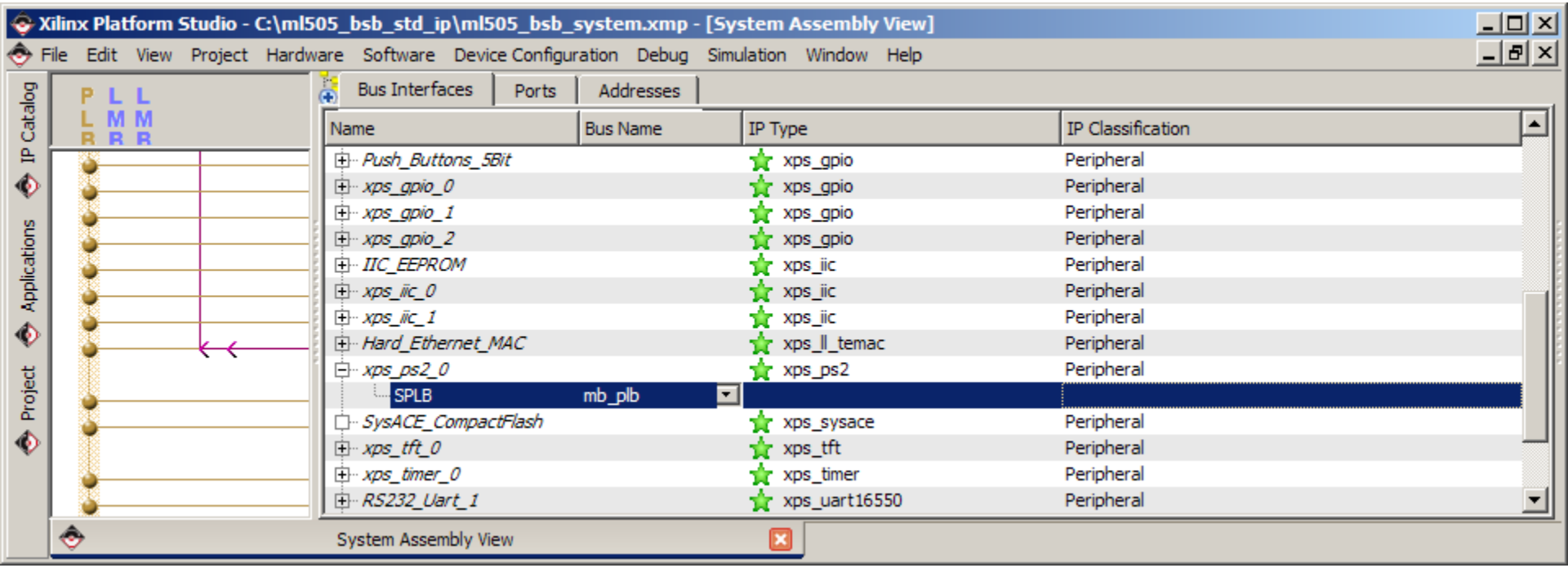
- **Expand these instances:**
  - **xps_gpio_0, xps_gpio_1, xps_gpio_3, xps_iic_0,** and **xps_iic_1**
  - Connect them to **mb_plb**



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Connect Buses

- **Expand this instance:**
  - **xps_ps2_0**
  - Connect it to **mb_plb**

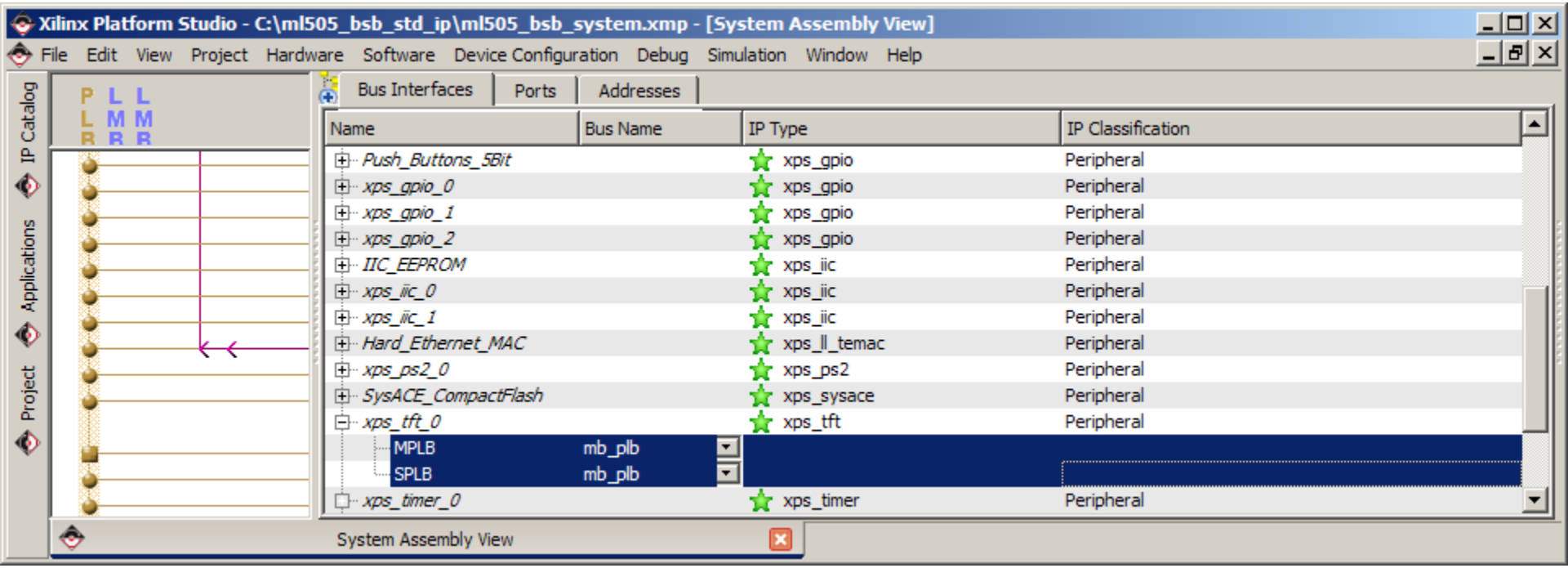


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Connect Buses

- **Expand this instance:**
  - **xps_tft_0**
  - Connect both the **MPLB** and the **SPLB** to **mb_plb**



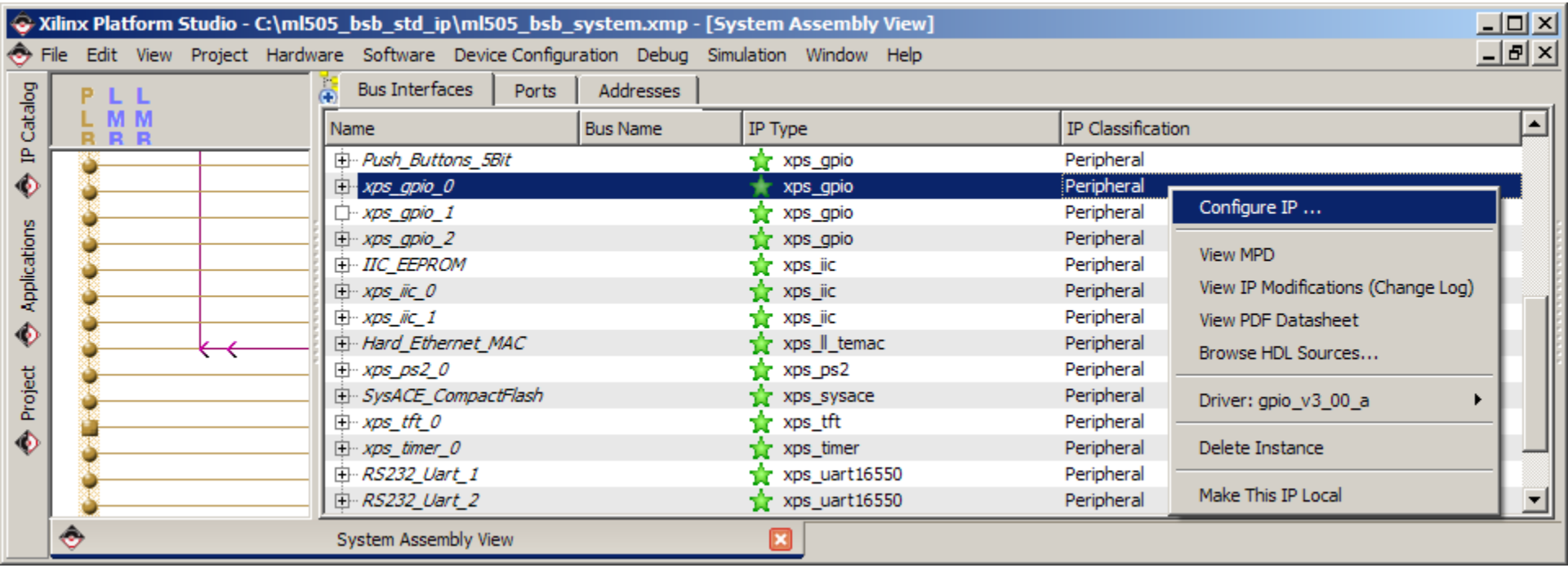
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IP Configuration

Configure IP

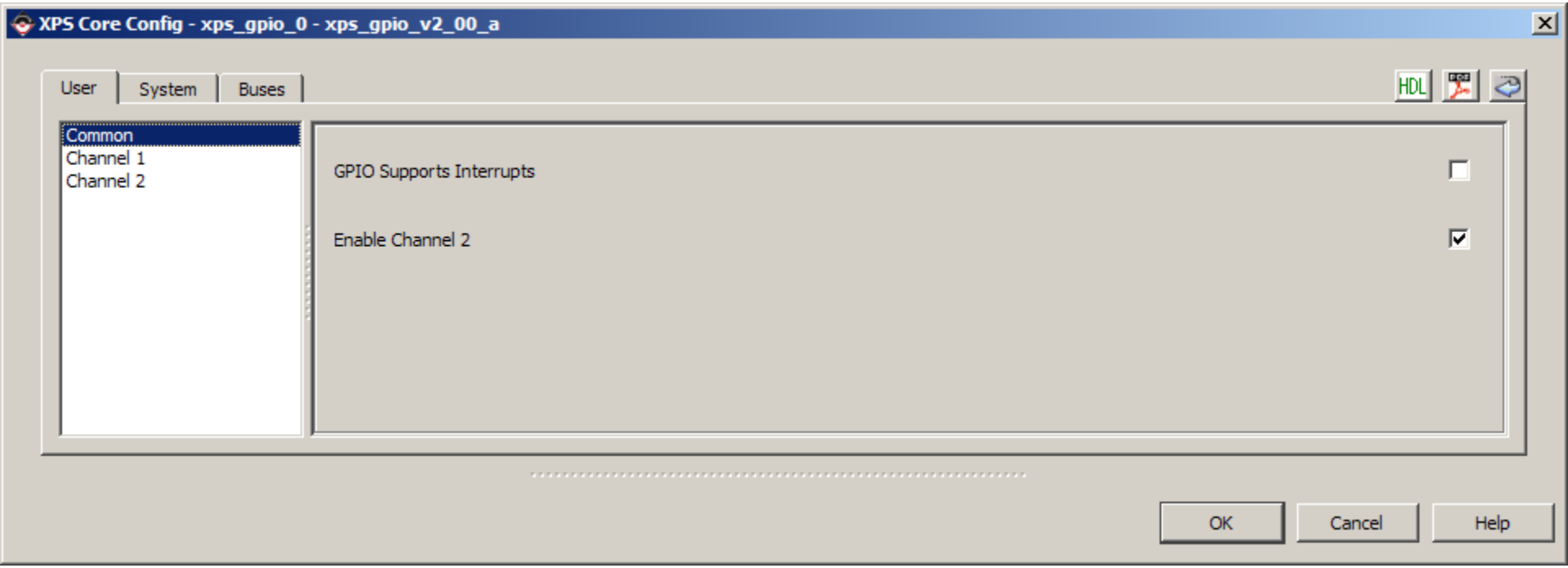
- **Configure the GPIO IP**
  - Right-click on the **xps_gpio_0**
  - Select **Configure IP…**



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Configure IP

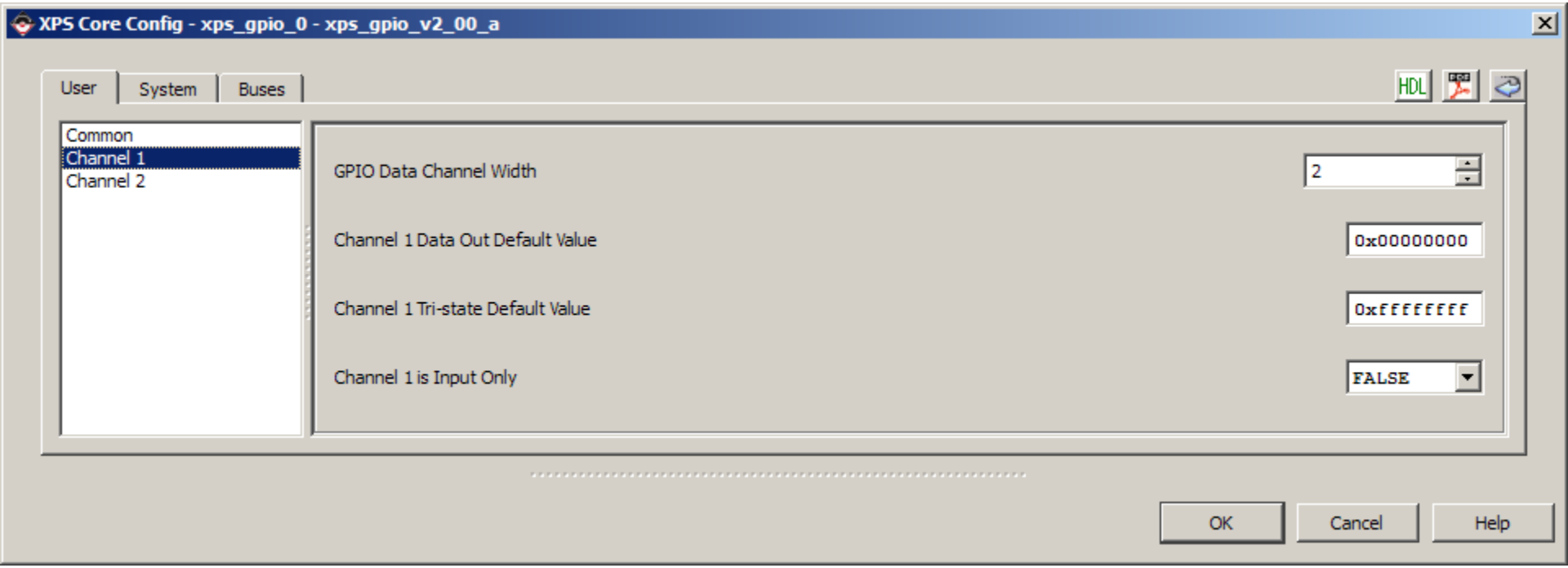
- **Under the User tab:**
  - Select **Common**
  - Check **Enable Channel 2**



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Configure IP

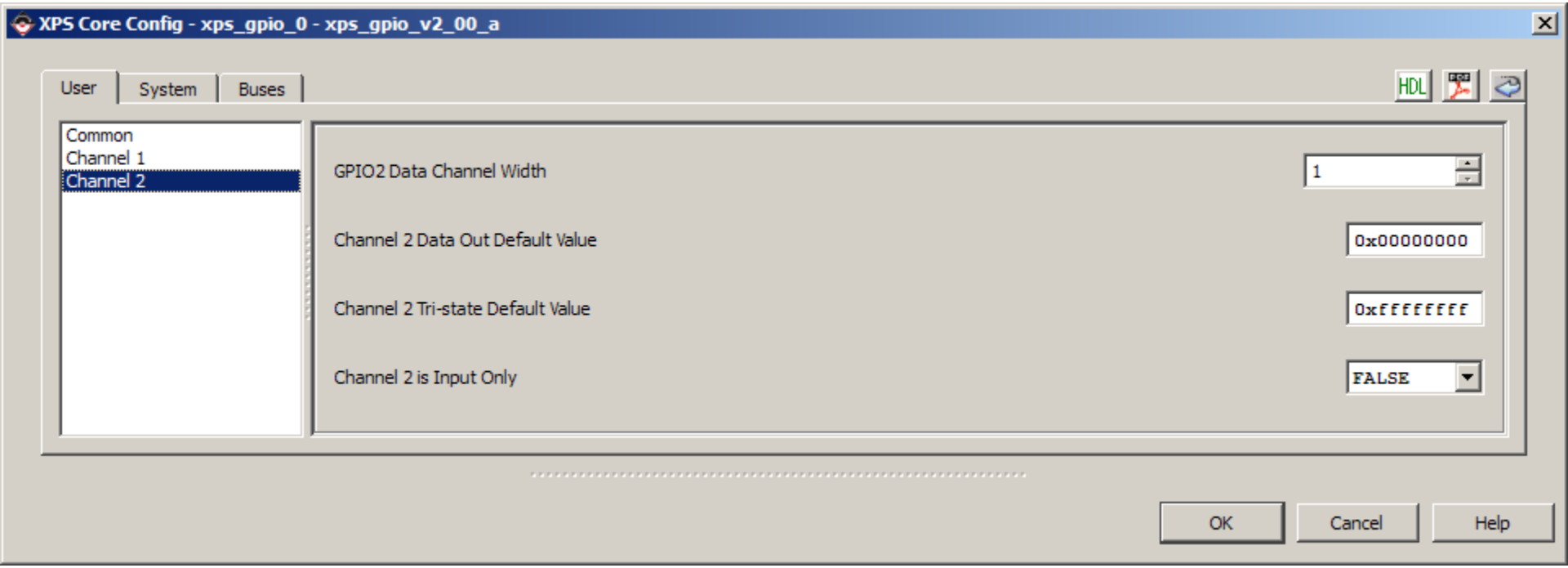
- **Under the User tab:**
  - Select **Channel 1**
  - Set GPIO2 Data Channel Width to **2** (Error LEDs)



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Configure IP

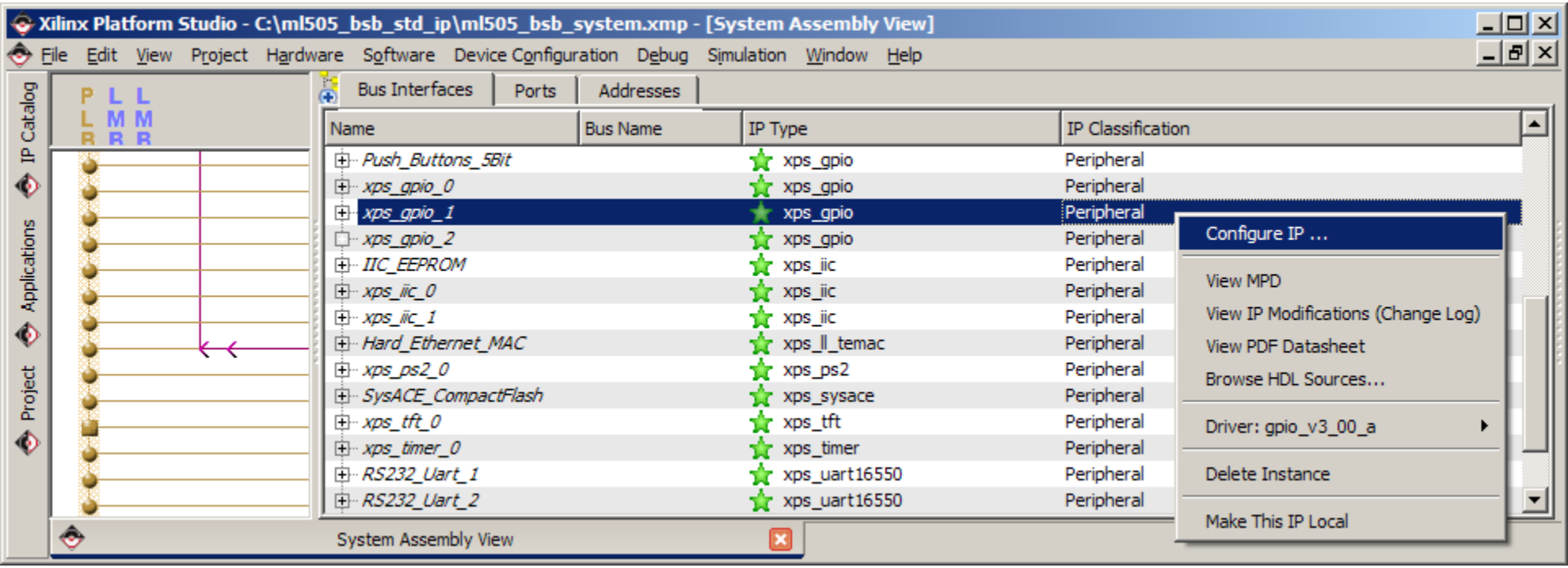
- **Under the User tab:**
  - Select **Channel 2**
  - Set GPIO2 Data Channel Width to **1** (Piezo transducer)



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Configure IP

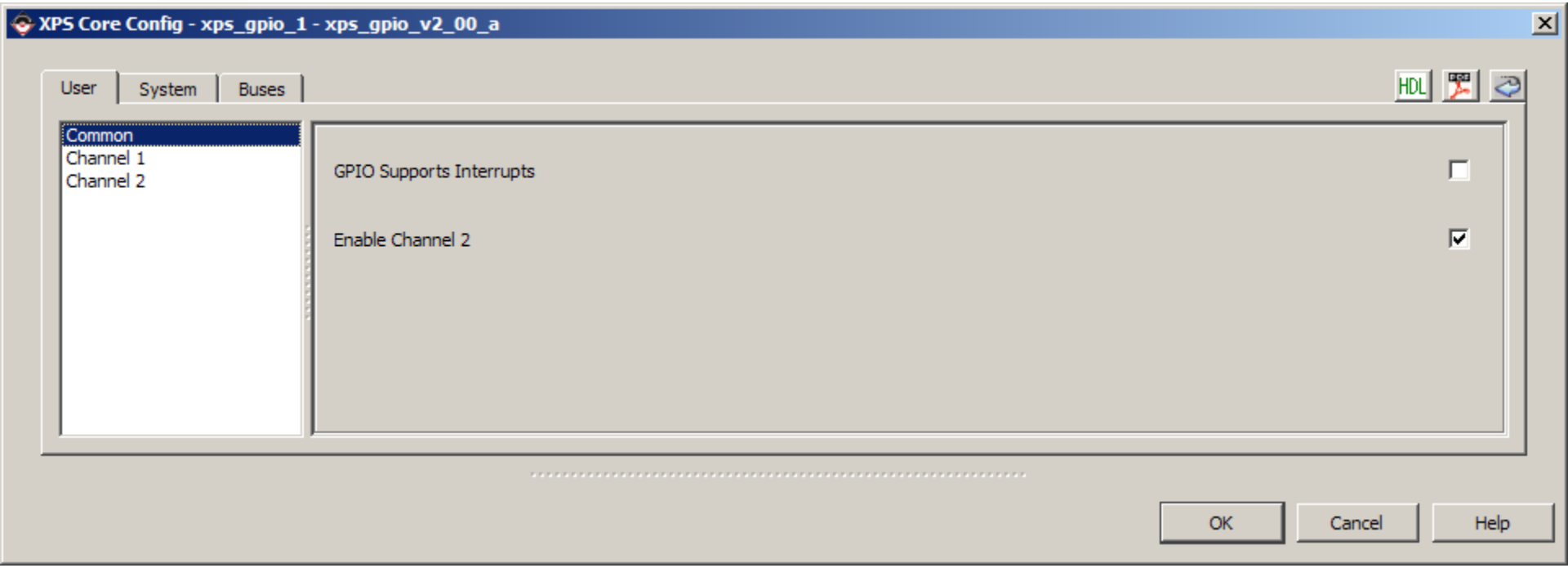
- **Configure the GPIO IP**
  - Right-click on the **xps_gpio_1**
  - Select **Configure IP…**



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Configure IP

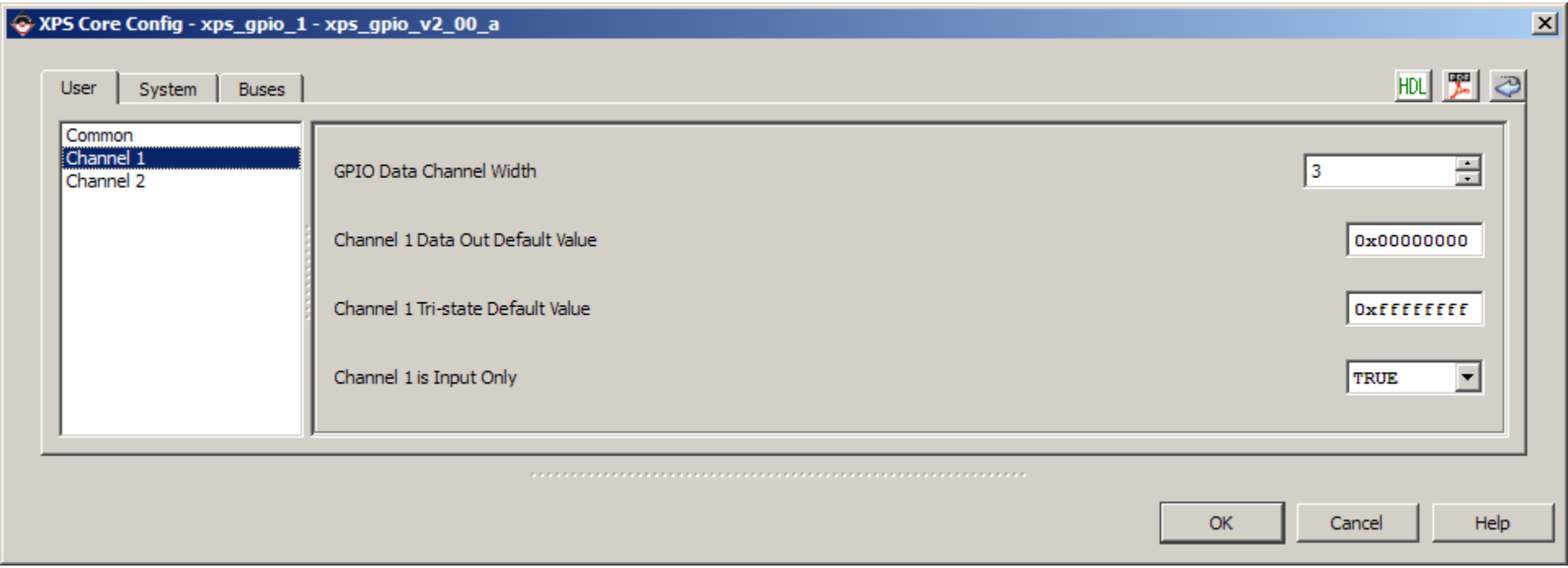
- **Under the User tab:**
  - Select **Common**
  - Check **Enable Channel 2**



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Configure IP

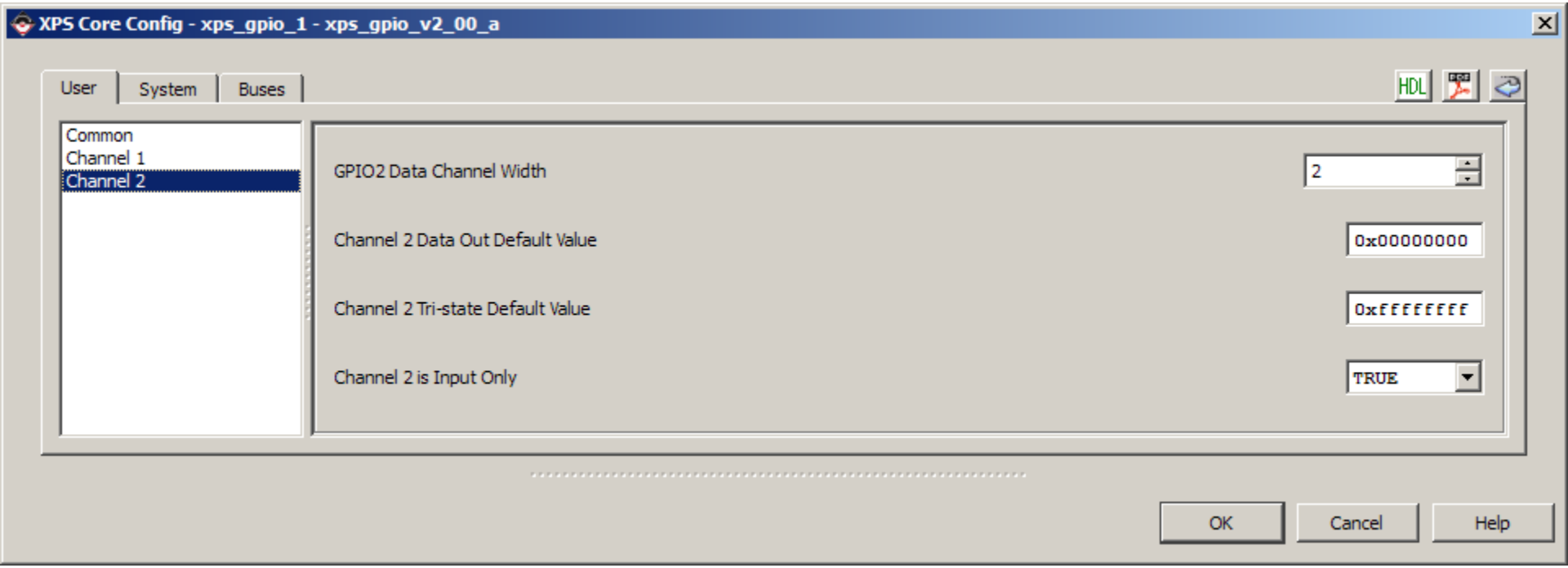
- **Under the User tab:**
  - Select **Channel 1**
  - Set GPIO2 Data Channel Width to **3** (Rotary Encoder/Push Button)
  - Set Channel 1 is Input Only to **TRUE**



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Configure IP

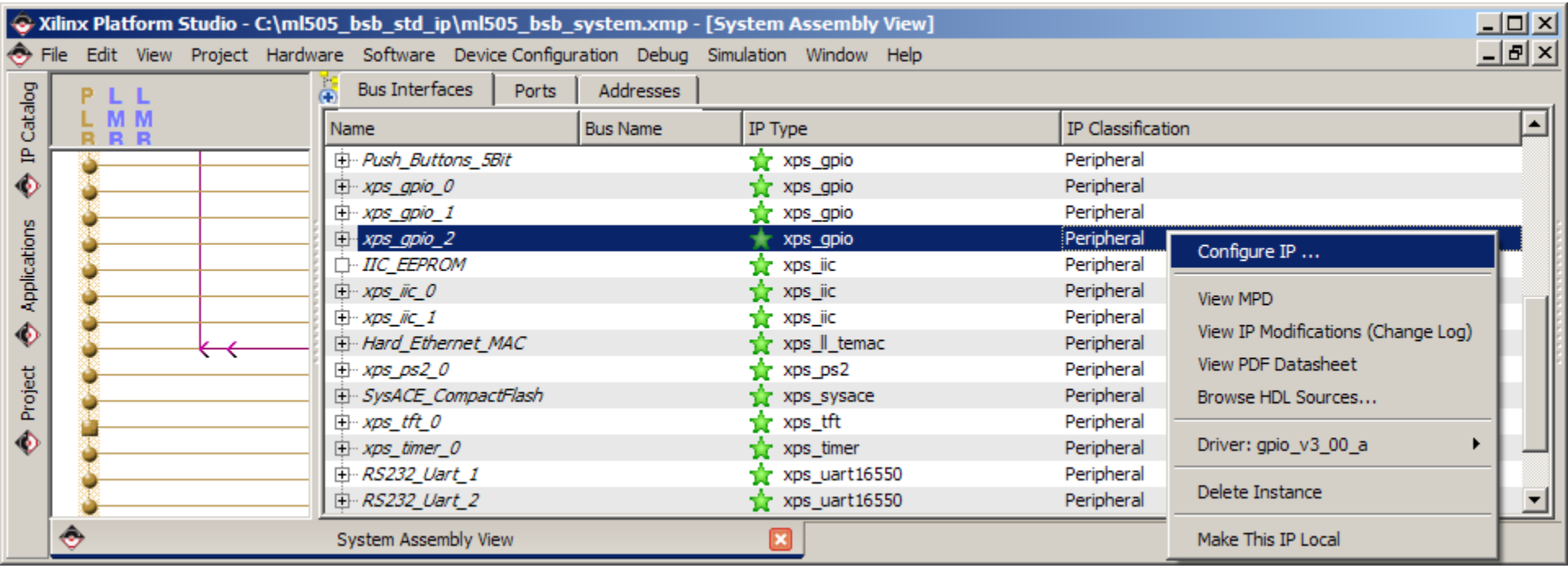
- **Under the User tab:**
  - Select **Channel 2**
  - Set GPIO2 Data Channel Width to **2** (SMA Diff CLK In)
  - Set Channel 2 is Input Only to **TRUE**



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Configure IP

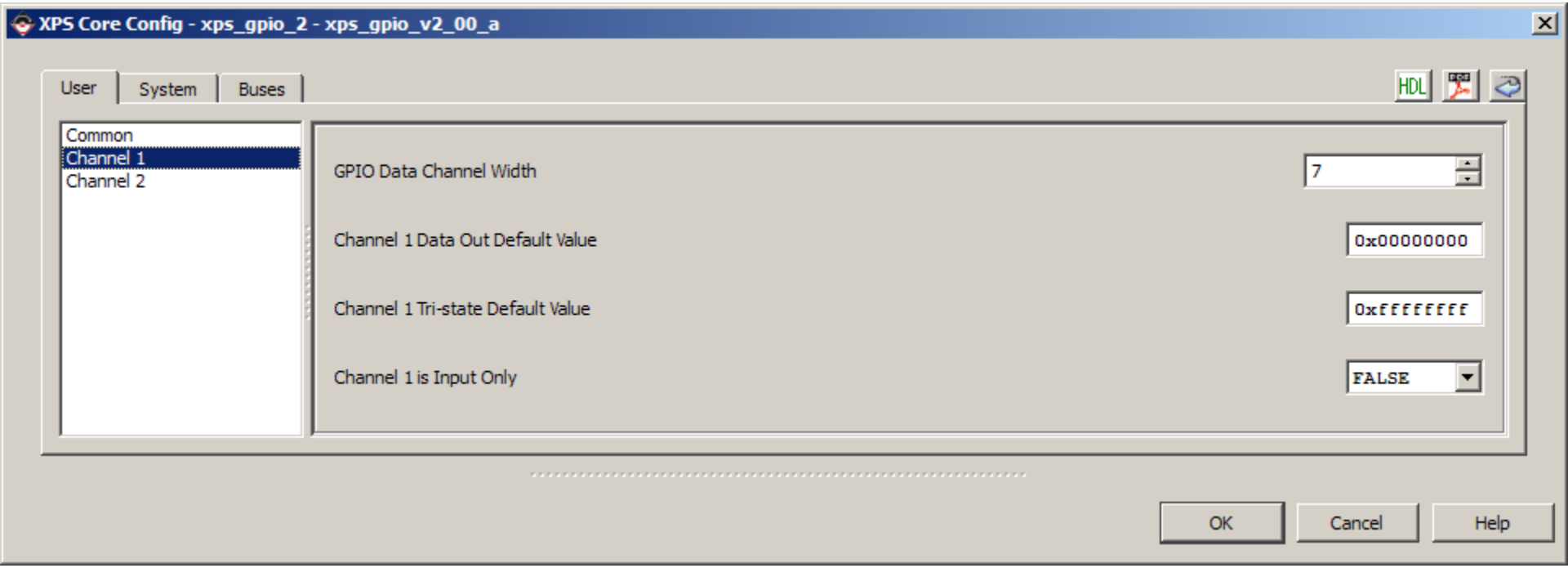
- **Configure the GPIO IP**
  - Right-click on the **xps_gpio_2**
  - Select **Configure IP…**



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Configure IP

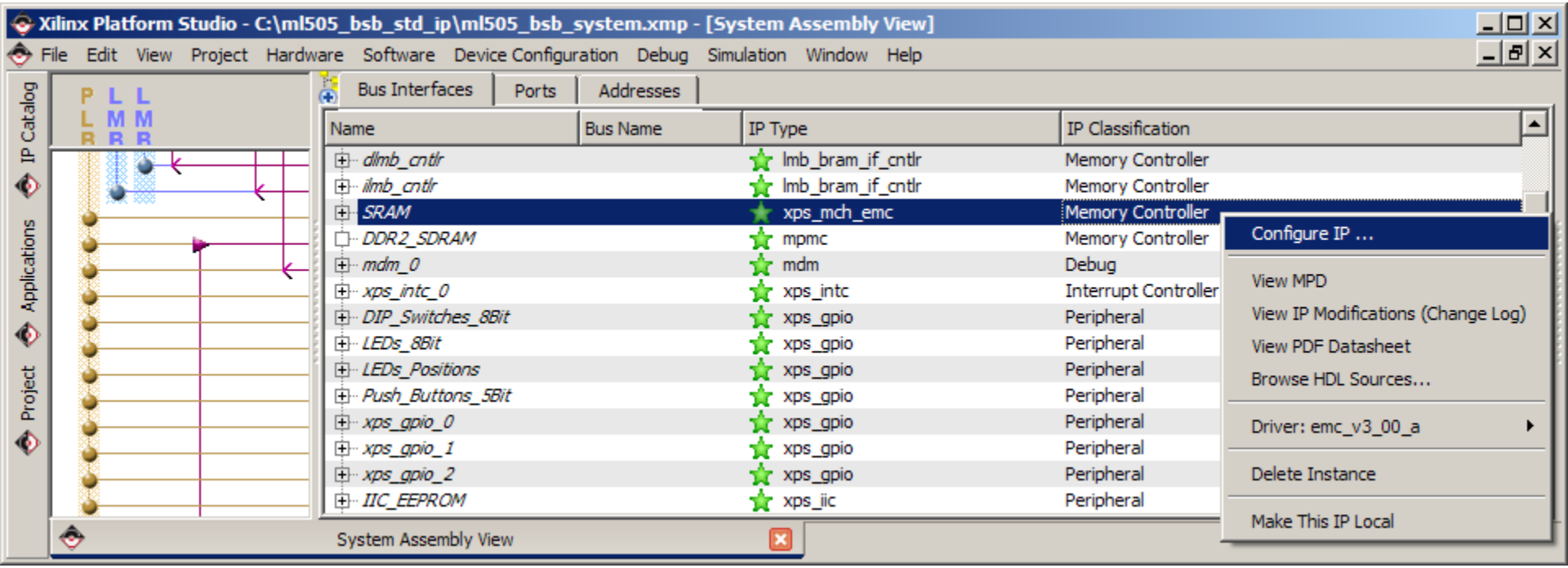
- **Under the User tab:**
  - Select **Channel 1**
  - Set GPIO2 Data Channel Width to **7** (LCD Display)



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Configure IP

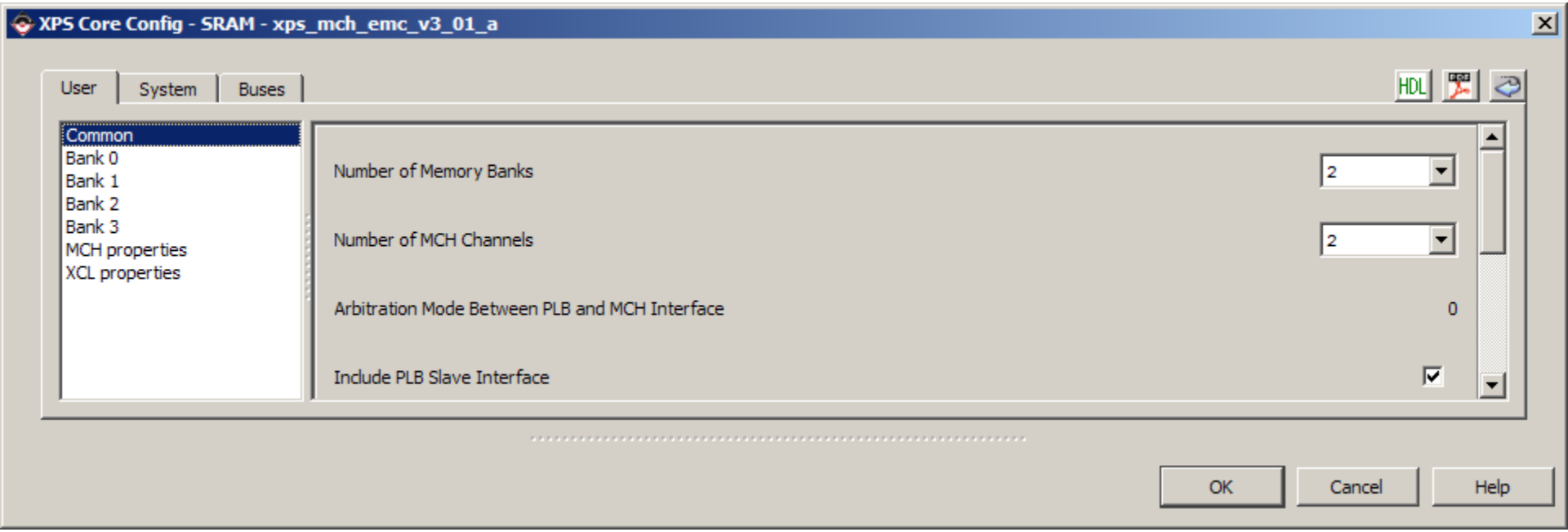
- **Configure the SRAM**
  - Right-click on the **SRAM**
  - Select **Configure IP…**



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Configure IP

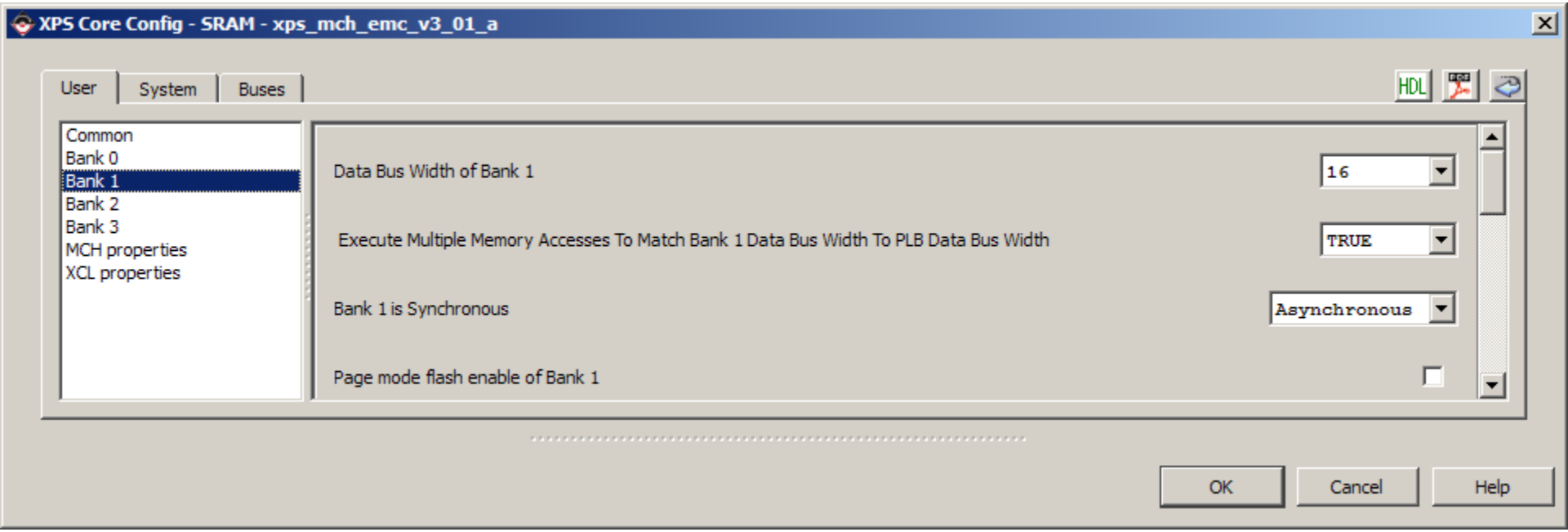
- **Under the User tab:**
  - Select **Common**
  - Set Number of Memory Banks to **2**
  - Set number of MCH Channels to **2**



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Configure IP

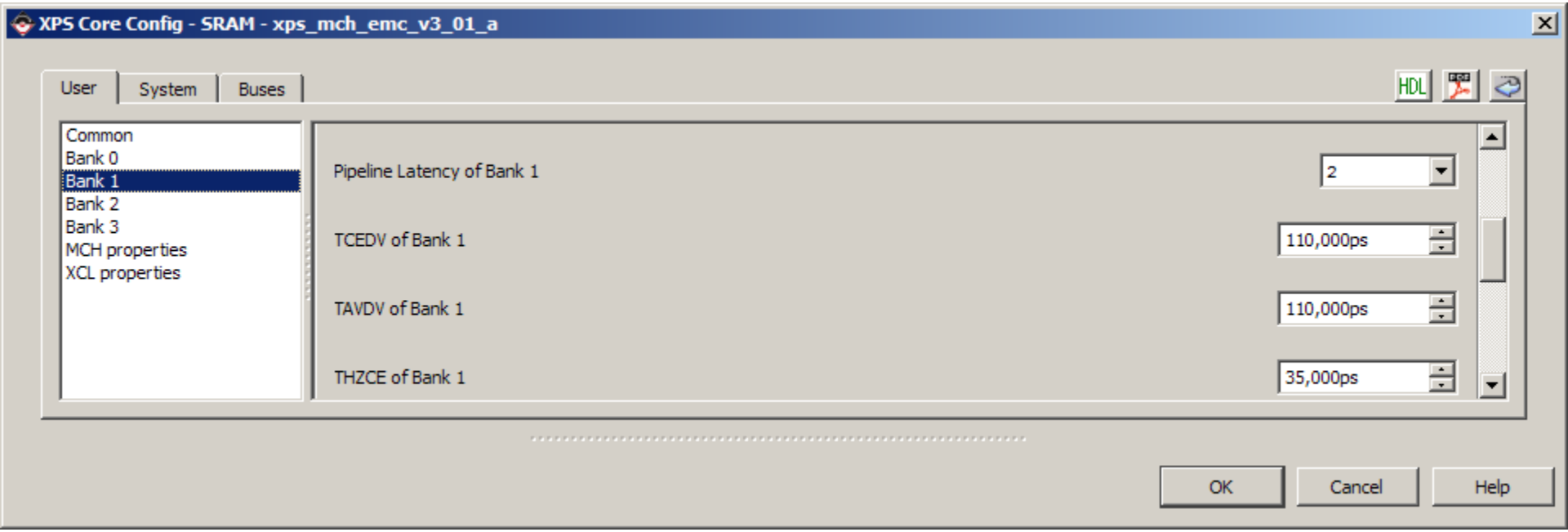
- **Under the User tab:**
  - Select **Bank 1**
  - Set Data Bus Width of Bank 1 to **16**
  - Set Data Width Matching to **True**



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Configure IP

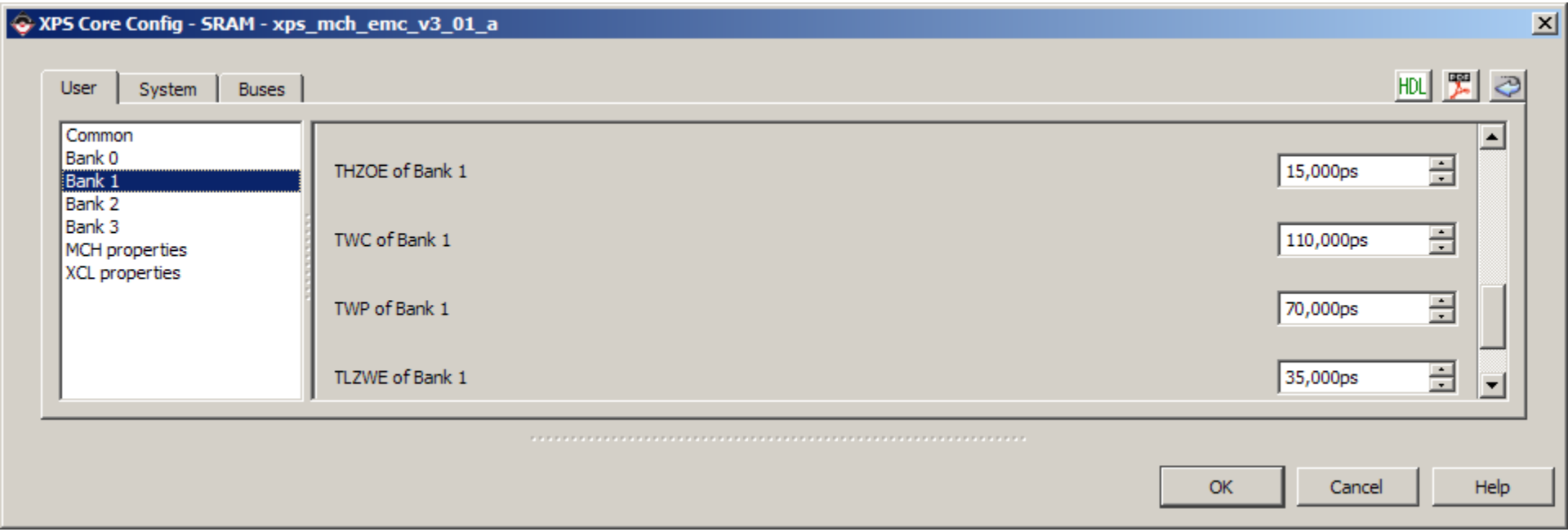
- **Under the User tab, Bank 1:**
  - Set TCEDV and TAVDV to: **110000**
  - Set THZCE to: **35000**



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Configure IP

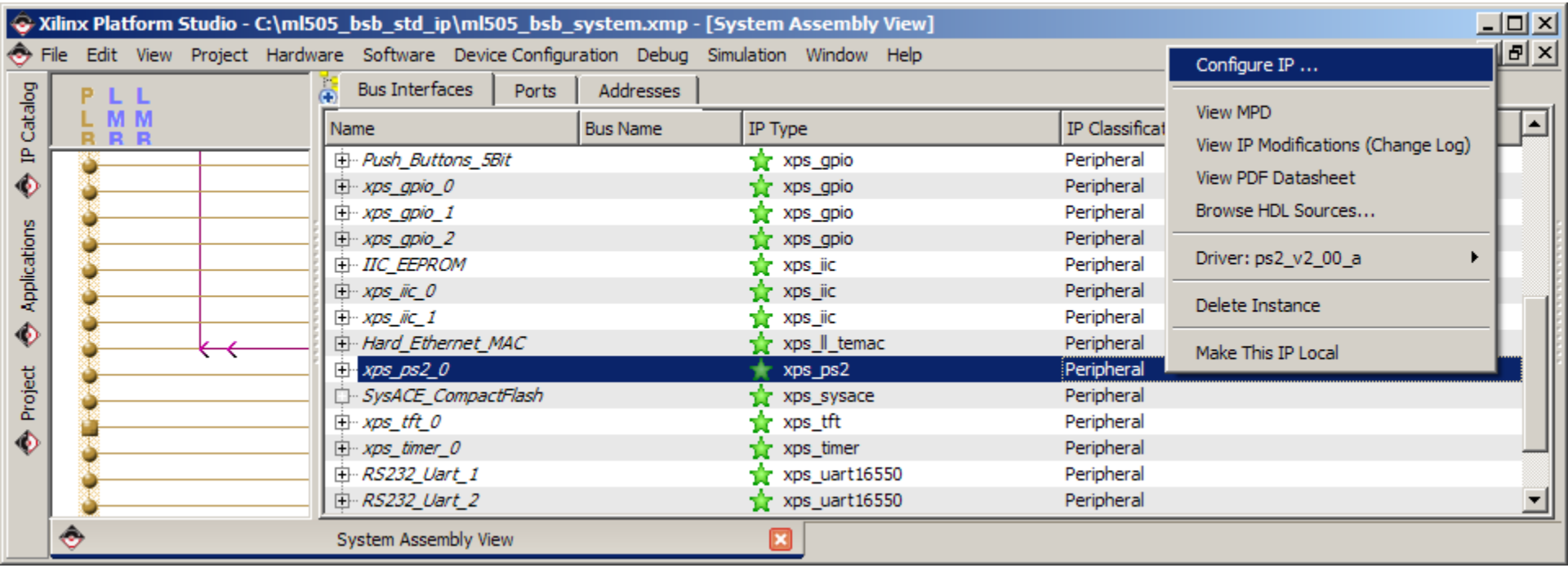
- **Under the User tab, Bank 1:**
  - Set THZOE to: **15000**
  - Set TWC to: **110000**
  - Set TWP to: **70000**
  - Set TLZWE to: **35000**



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Configure IP

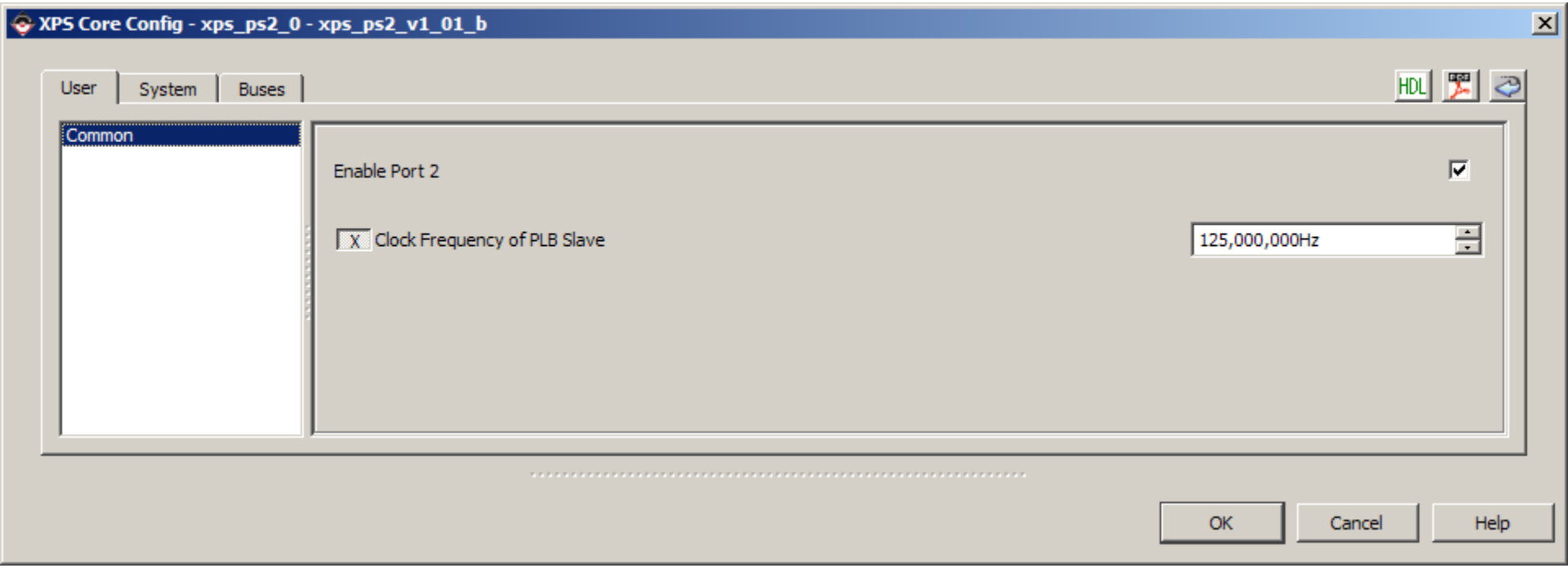
- **Configure the PS/2 Interface**
  - Right-click on the **xps_ps2_0**
  - Select **Configure IP…**



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Configure IP

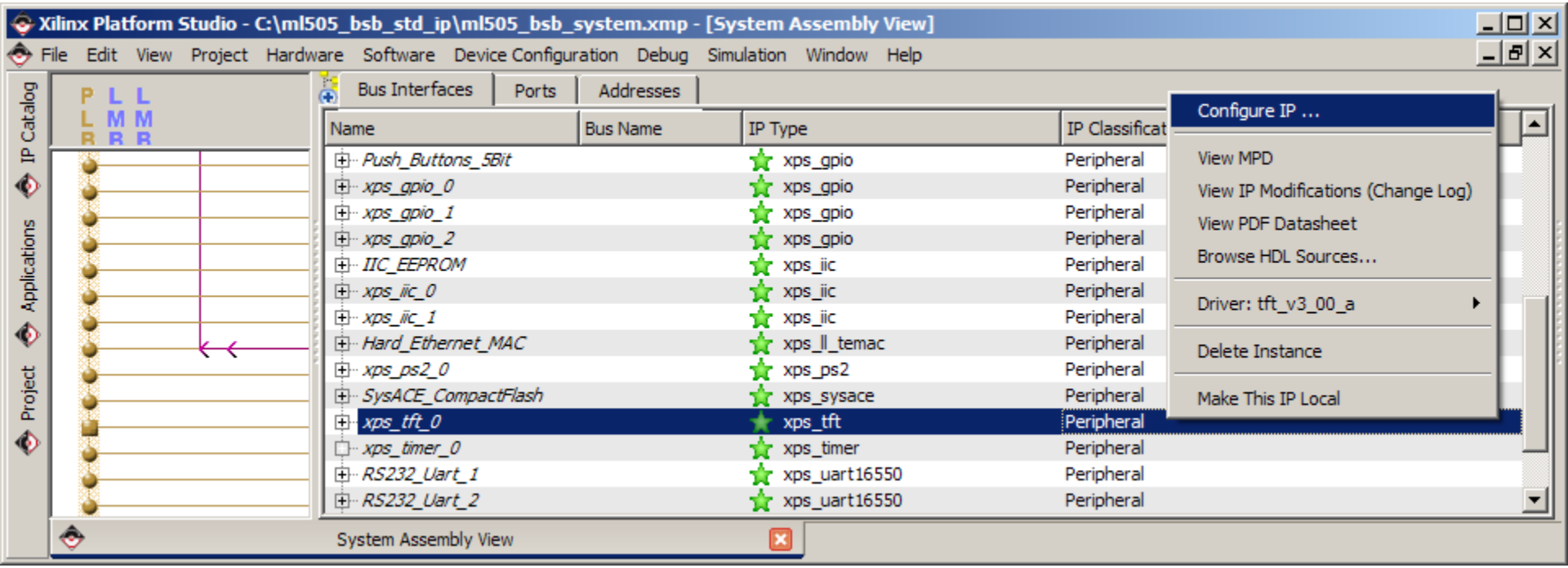
- **Under the User tab:**
  - Select **Common**
  - Check **Enable Port 2**



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Configure IP

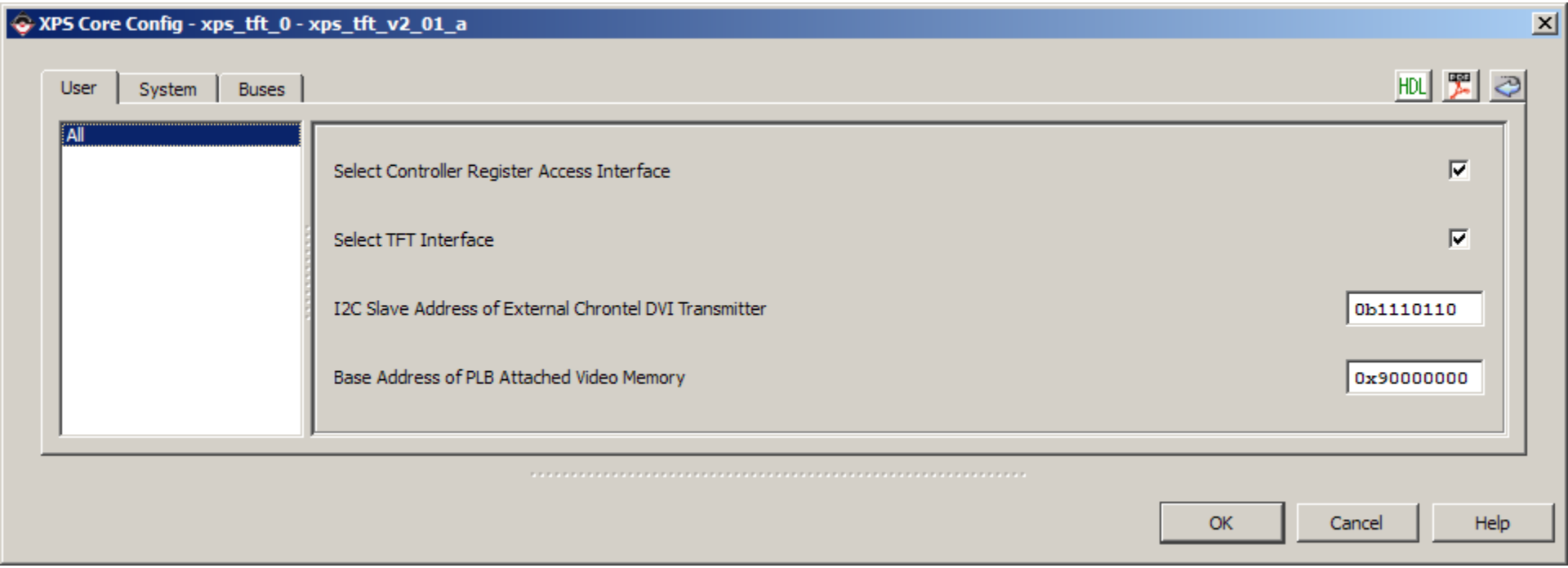
- **Configure the DVI Interface**
  - Right-click on the **xps_tft_0**
  - Select **Configure IP…**



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Configure IP

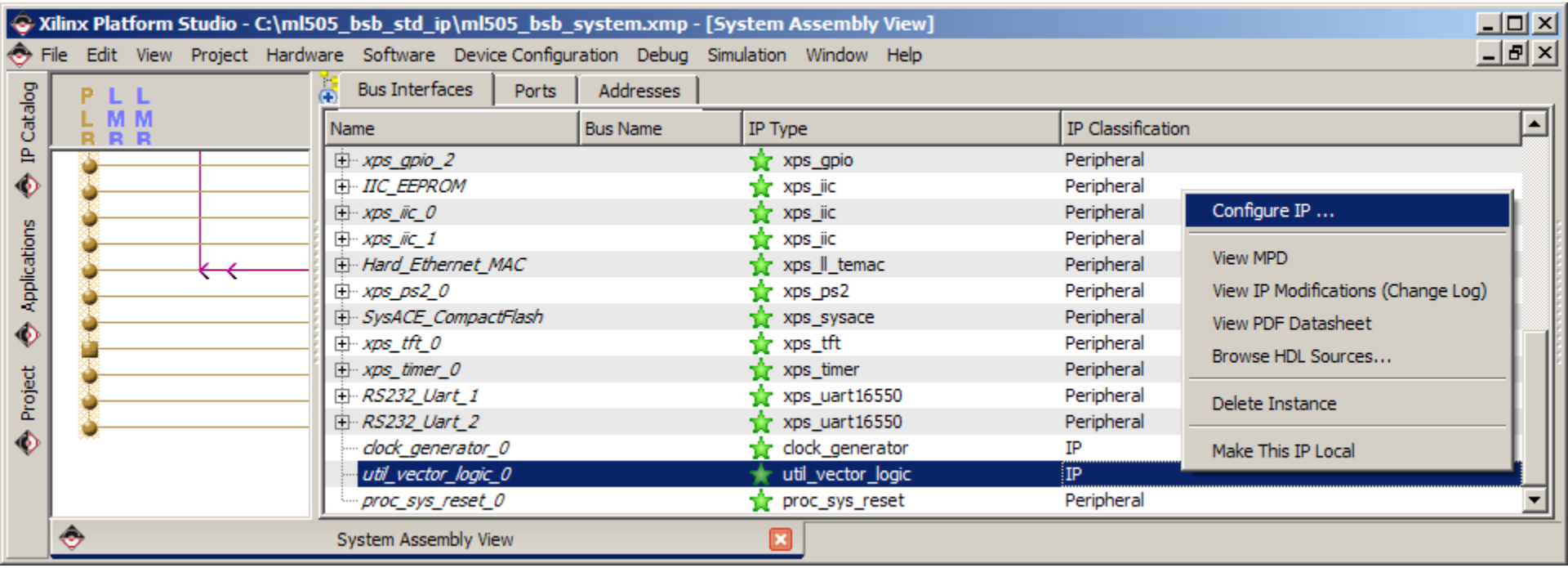
- **Under the User tab:**
  - Select **All**
  - Set Base Address of PLB Attached Video Memory to **0x90000000**



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Configure IP

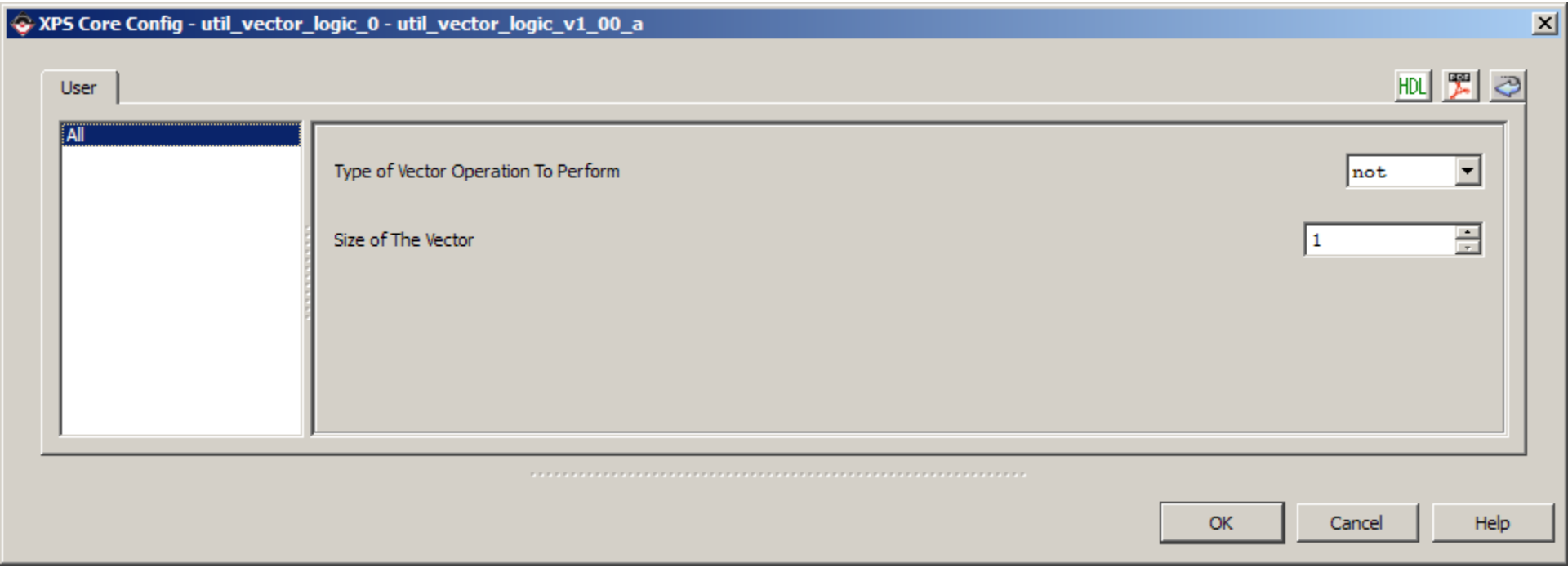
- **Configure the Utility Vector Logic**
  - Right-click on the **util_vector_logic_0**
  - Select **Configure IP…**



Note: Presentation applies to the ML505, ML506, and ML507

Configure IP

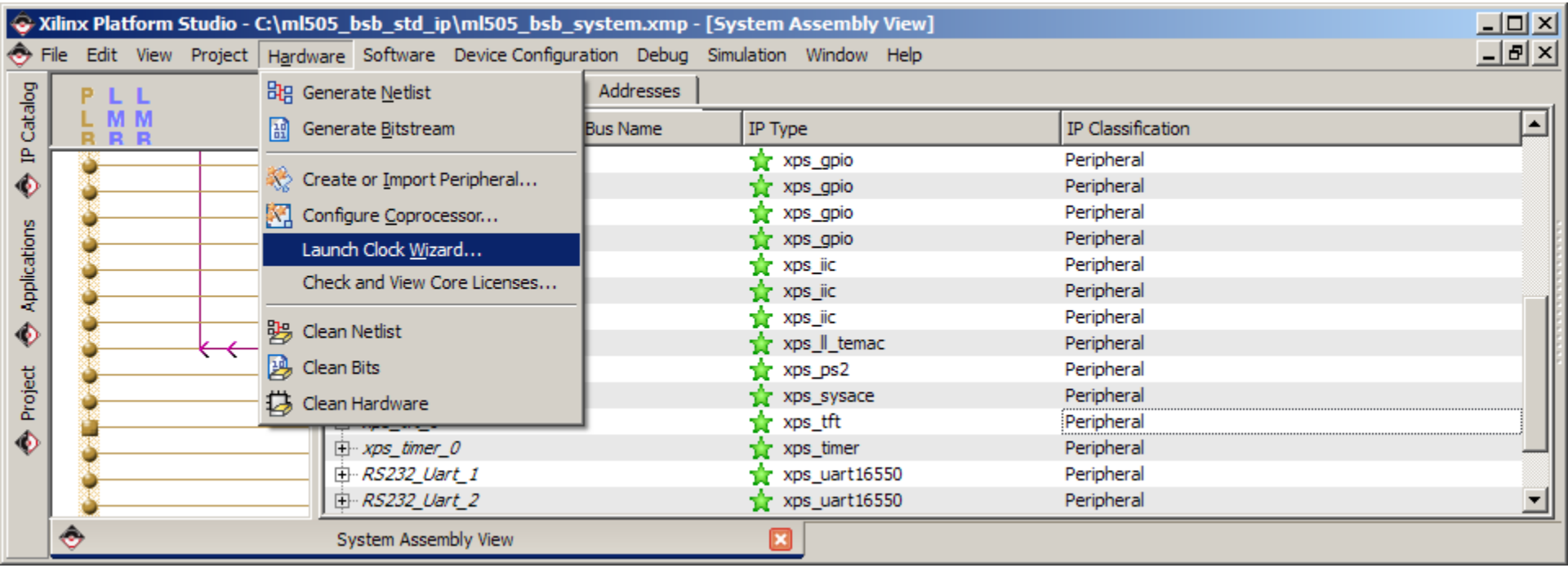
- **Under the User tab:**
  - Select **All**
  - Set Type of Vector Operation To Perform to **not**
  - Set Size of The Vector to **1**



Note: Presentation applies to the ML505, ML506, and ML507

Configure IP

- **Configure the Clock Generator**
  - Select **Hardware → Launch Clock Wizard…**

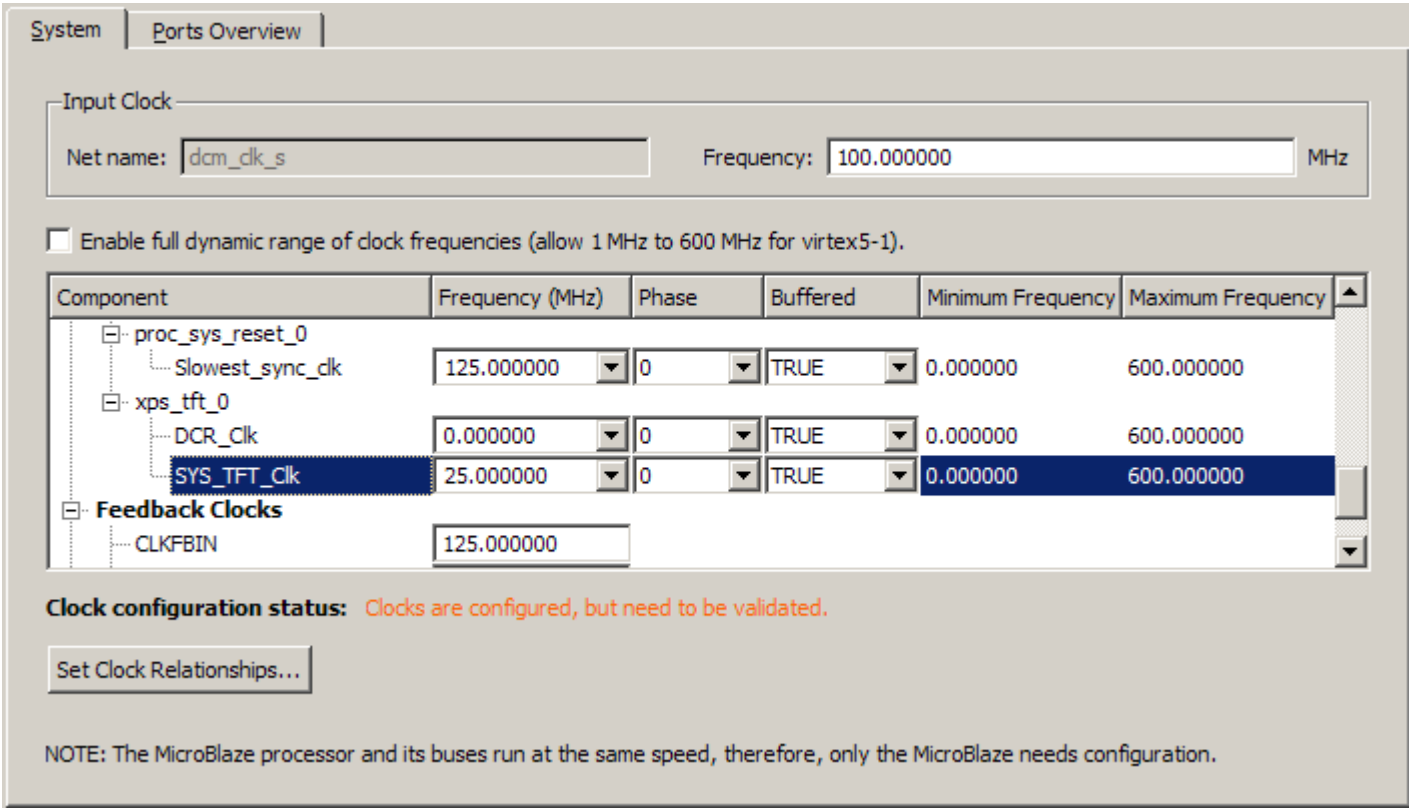


Note: Presentation applies to the ML505, ML506, and ML507

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Configure IP

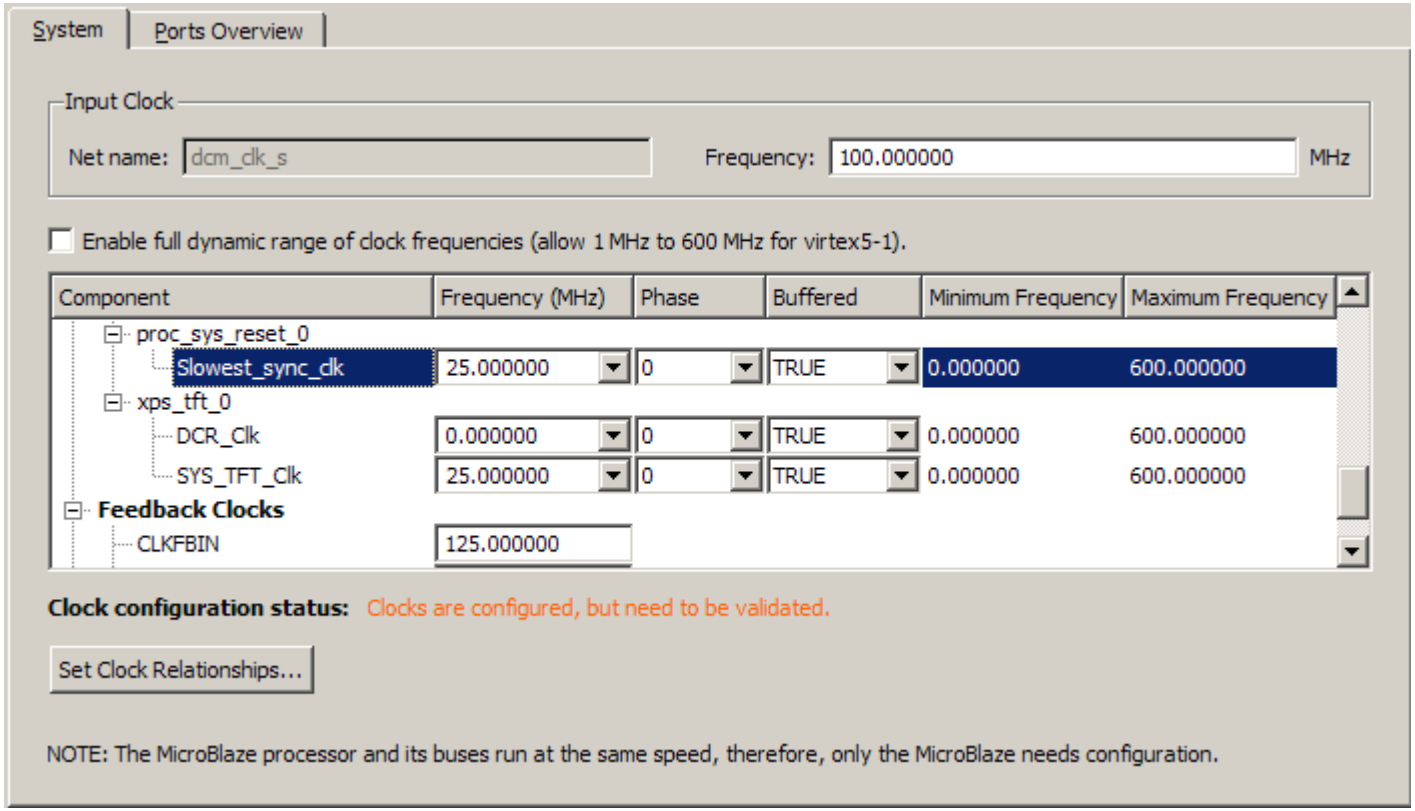
- **Under the System tab:**
  - Select **xps_tft_0 → SYS_TFT_Clk**
  - Set the frequency to **25 MHz**



Note: Presentation applies to the ML505, ML506, and ML507

Configure IP

- **Under the System tab:**
  - Select **proc_sys_reset_0 → Slowest_sync_clk**
  - Set the frequency to **25 MHz**



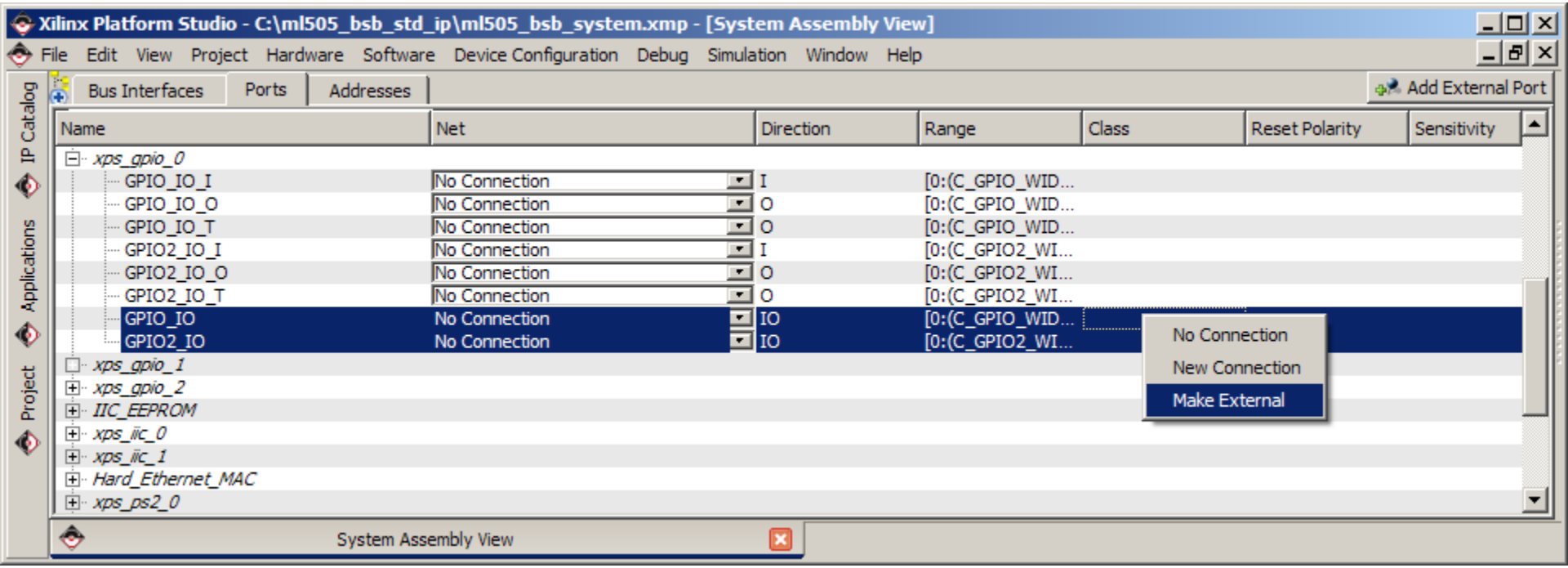
Note: Presentation applies to the ML505, ML506, and ML507

XILINX®

Connect IP Ports

Connect Ports

- **Select the Ports tab**
- **Expand this instance:**
  - **xps_gpio_0**
  - Select **Make External** for the **GPIO_IO** and **GPIO2_IO** ports

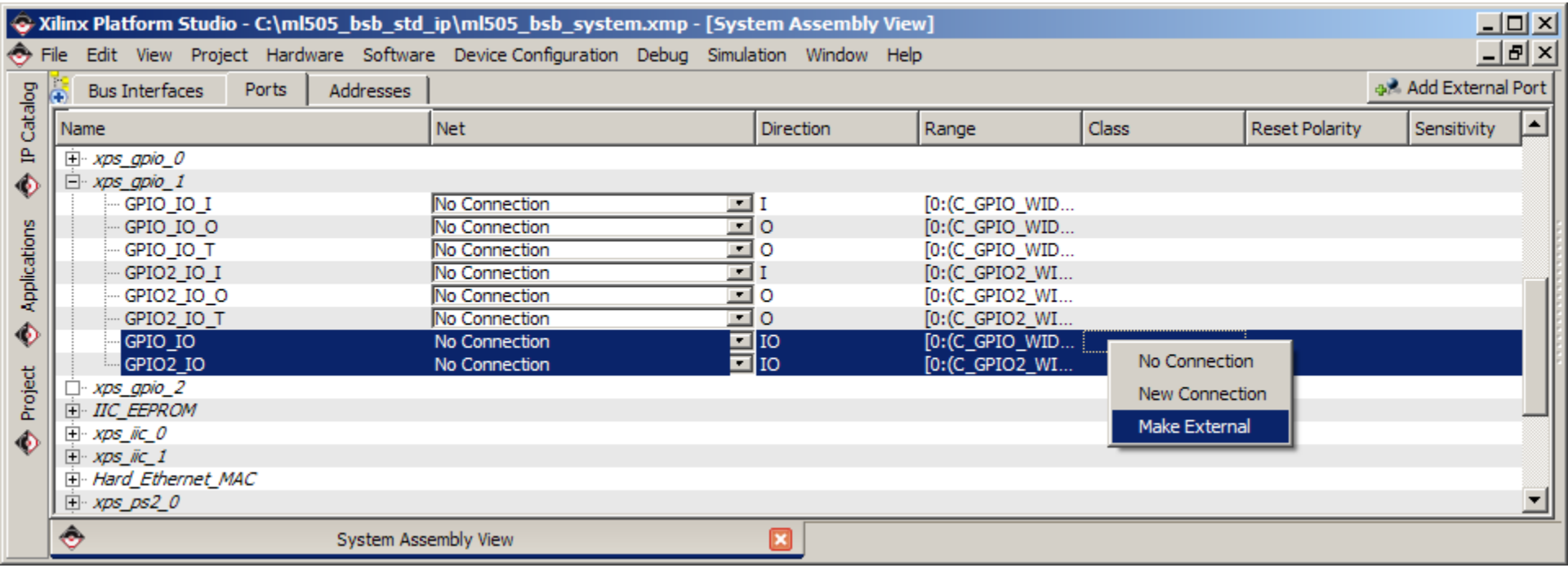


Note: Presentation applies to the ML505, ML506, and ML507

XILINX

Connect Ports

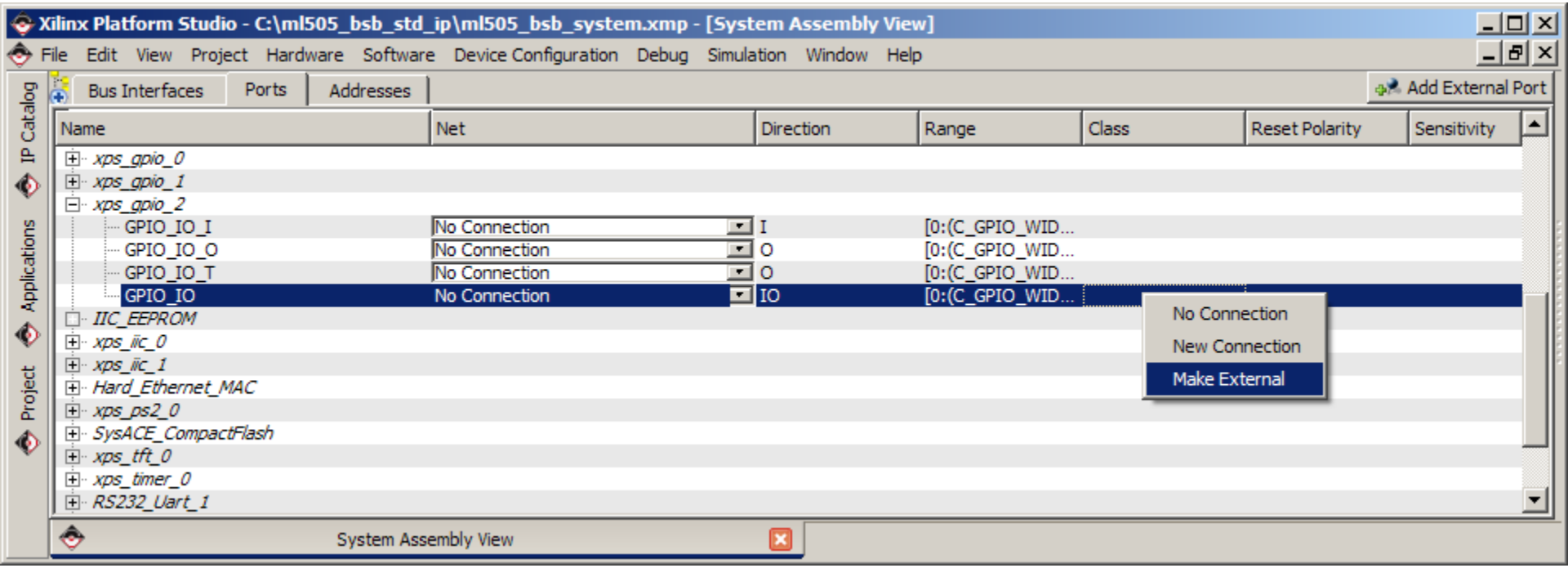
- **Expand this instance:**
  - **xps_gpio_1**
  - Select **Make External** for the **GPIO_IO** and **GPIO2_IO** ports



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

- **Expand this instance:**
  - **xps_gpio_2**
  - Select **Make External** for the **GPIO_IO** port

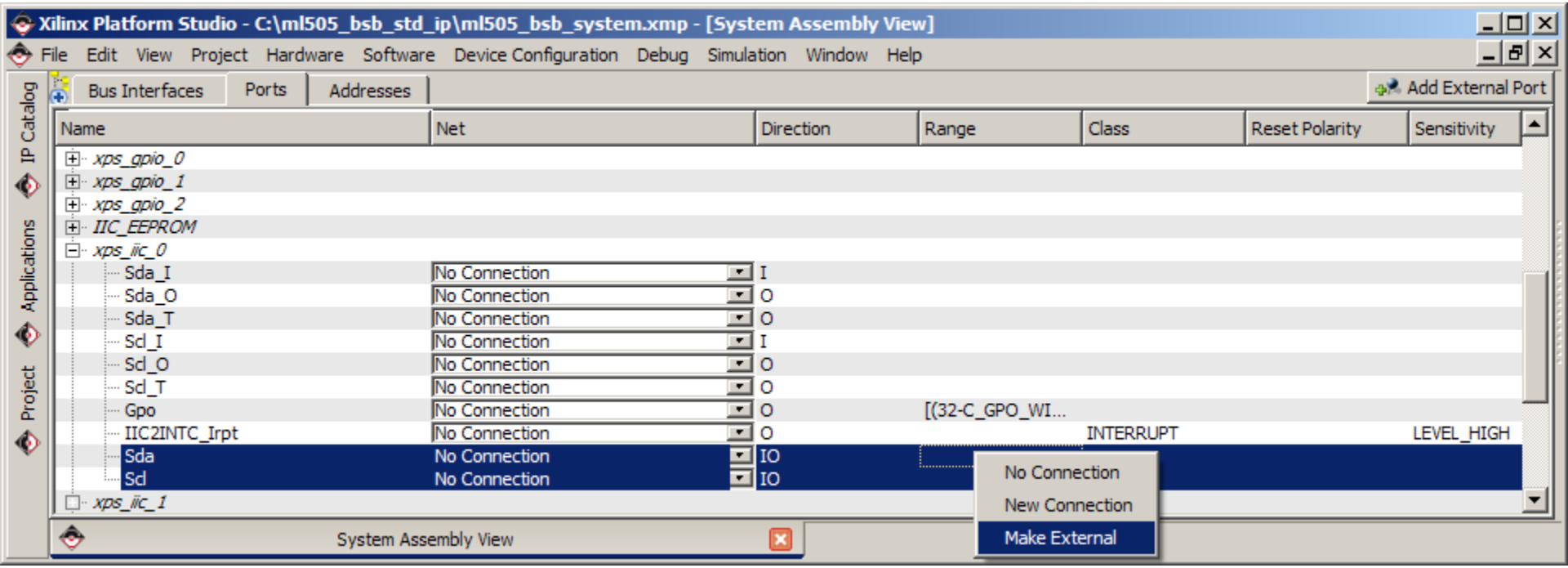


Note: Presentation applies to the ML505, ML506, and ML507

XILINX®

Connect Ports

- **Expand this instance:**
  - **xps_iic_0**
  - Select **Make External** for the **Sda** and **Scl** ports

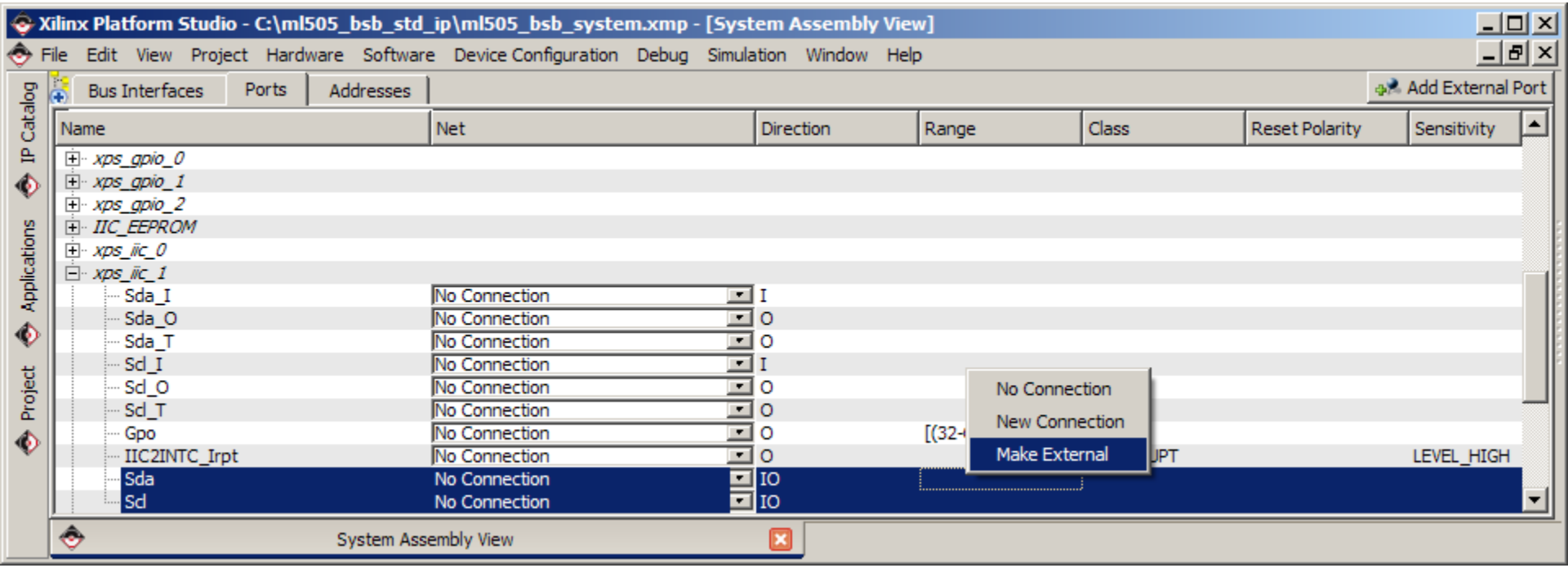


Note: Presentation applies to the ML505, ML506, and ML507

XILINX®

Connect Ports

- **Expand this instance:**
  - **xps_iic_1**
  - Select **Make External** for the **Sda** and **Scl** ports

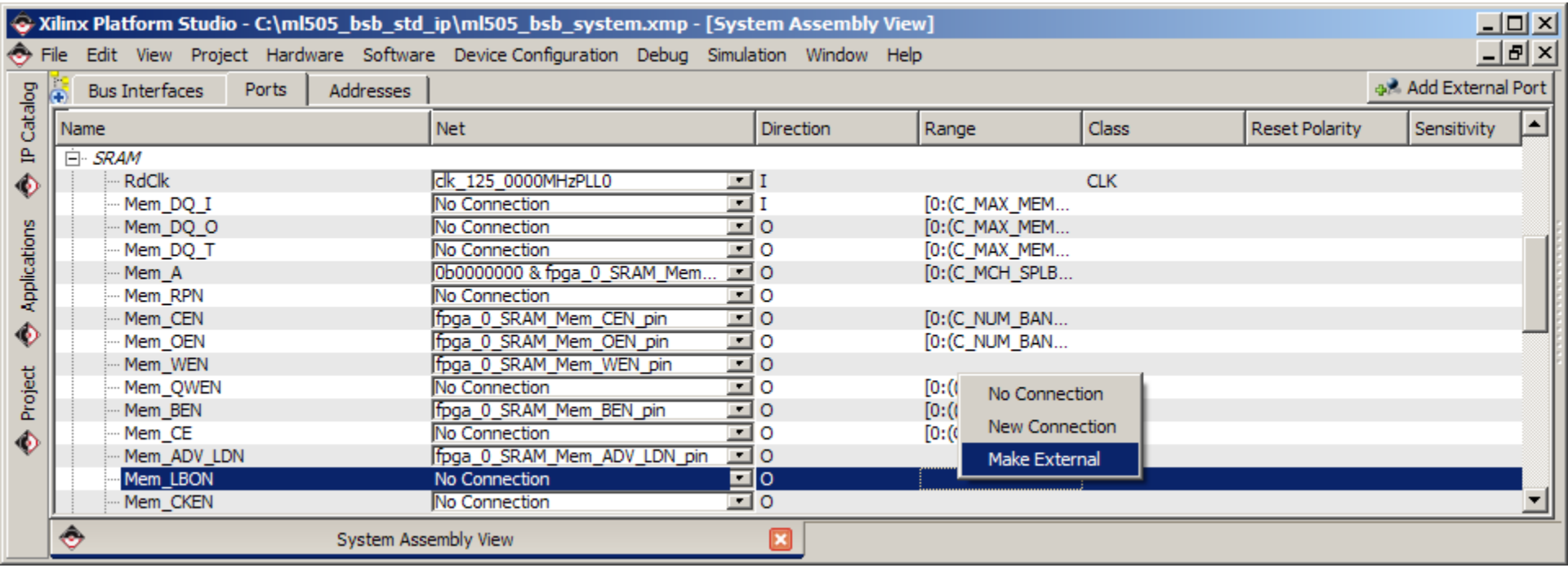


Note: Presentation applies to the ML505, ML506, and ML507

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Connect Ports

- **Expand this instance:**
  - **SRAM**
  - Select **Make External** for the **Mem_LBON** port

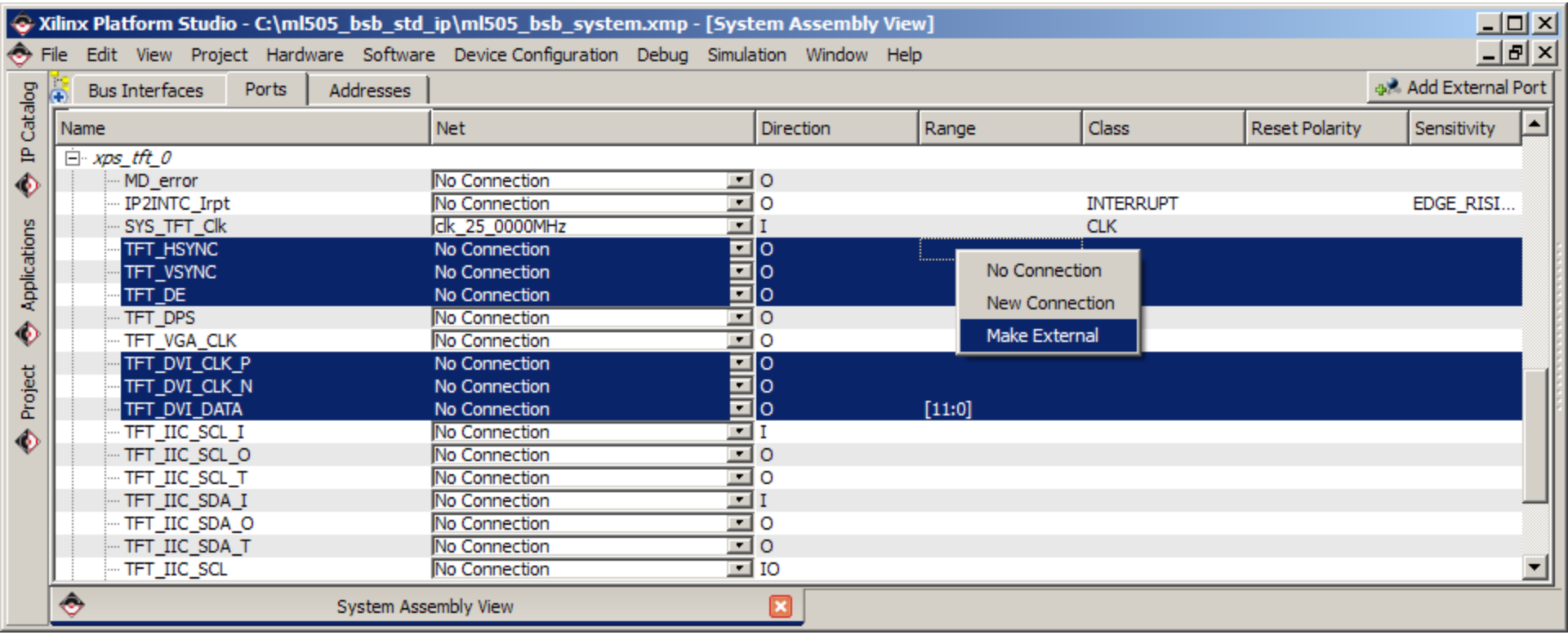


Note: Presentation applies to the ML505, ML506, and ML507

XILINX®

Connect Ports

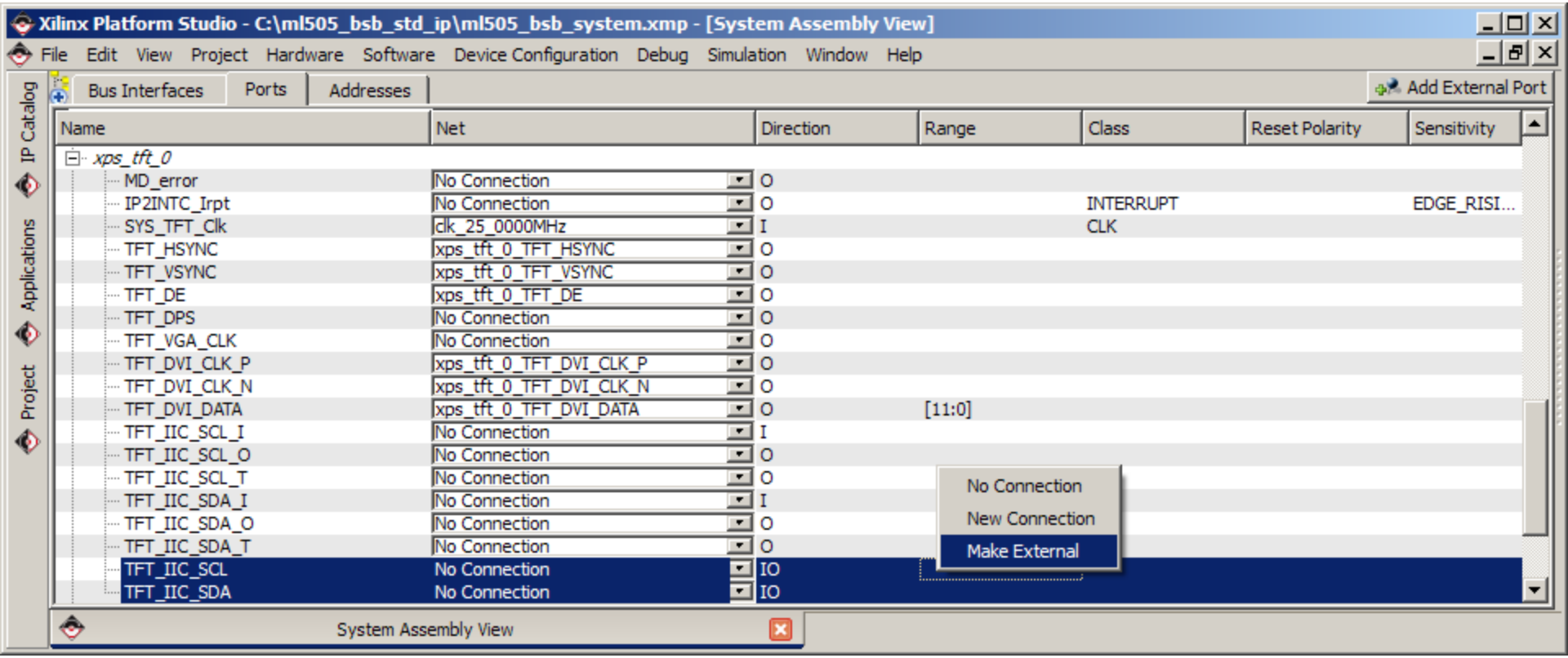
- **Expand this instance:**
  - **xps_tft_0**
  - Select **Make External** for **TFT_HSYNC**, **TFT_VSYNC**, **TFT_DE**, **TFT_DVI_CLK_P**, **TFT_DVI_CLK_N**, and **TFT_DVI_DATA**



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

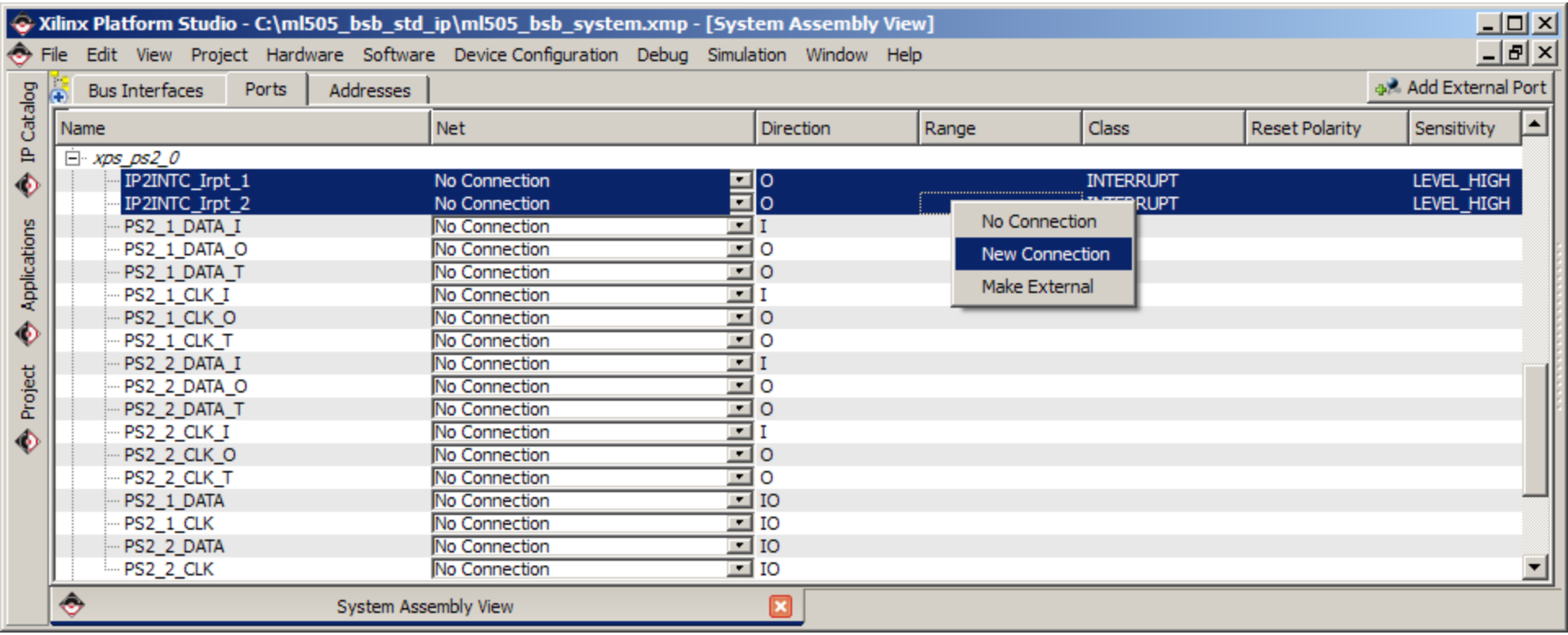
- **For instance xps_tft_0:**
  - Select **Make External** for **TFT_IIC_SCL** and **TFT_IIC_SDA** ports



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

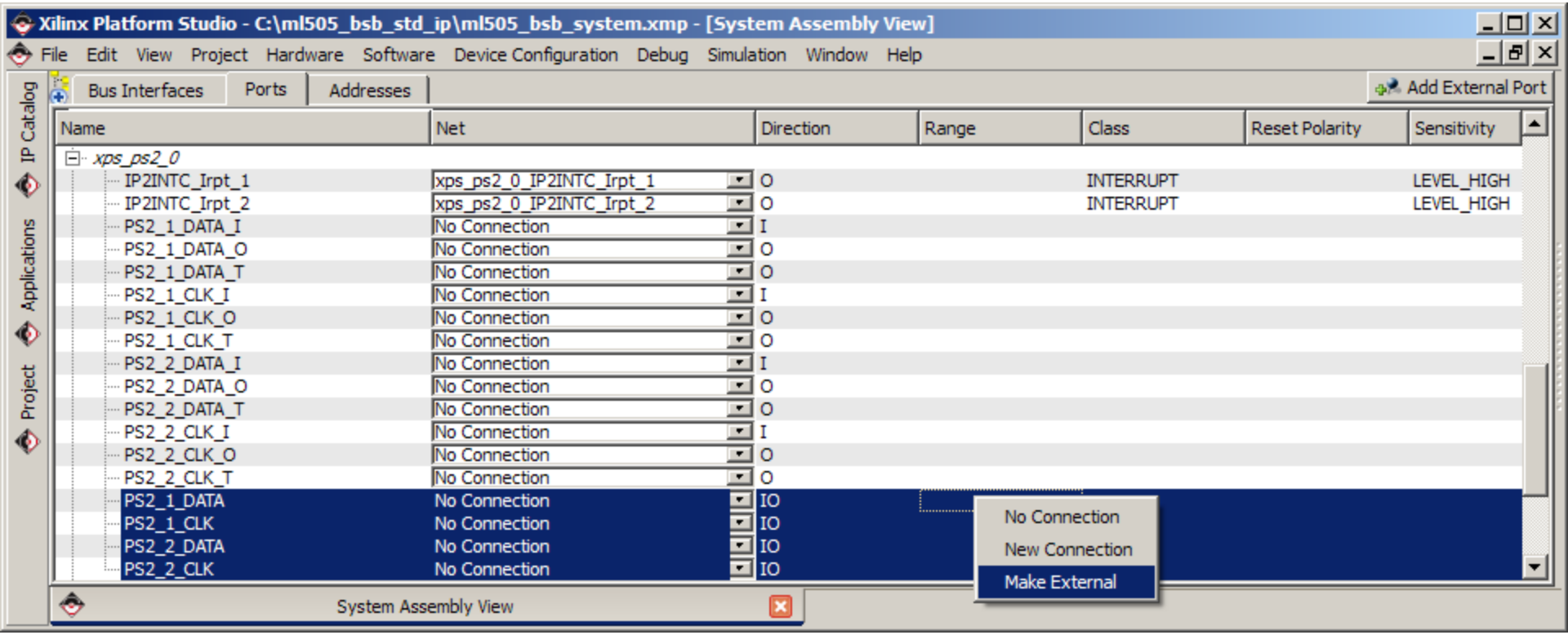
- **Expand this instance:**
  - **xps_ps2_0**
  - Select **New Connection** for **IP2INTC_Irpt_1** and **IP2INTC_Irpt_2** ports



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

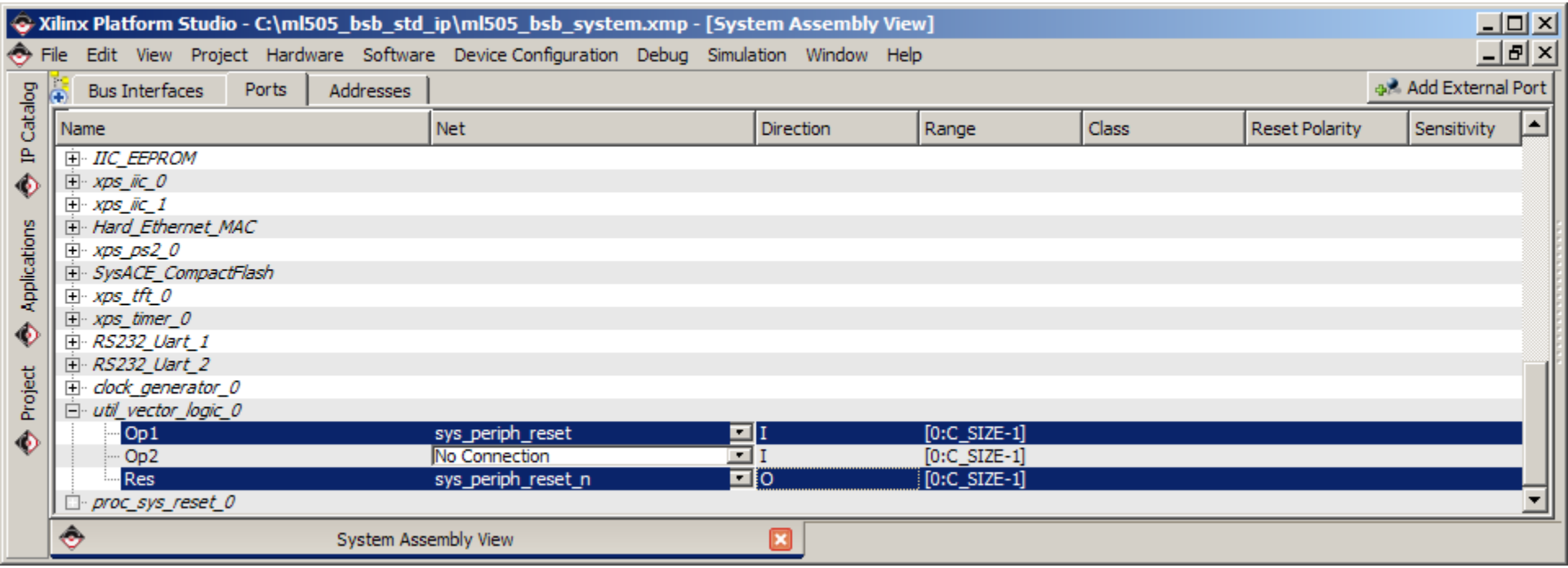
- **For instance xps_ps2_0:**
  - Select **Make External** for **PS2_1_DATA**, **PS2_1_CLK**, **PS2_2_DATA**, and **PS2_2_CLK** ports



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

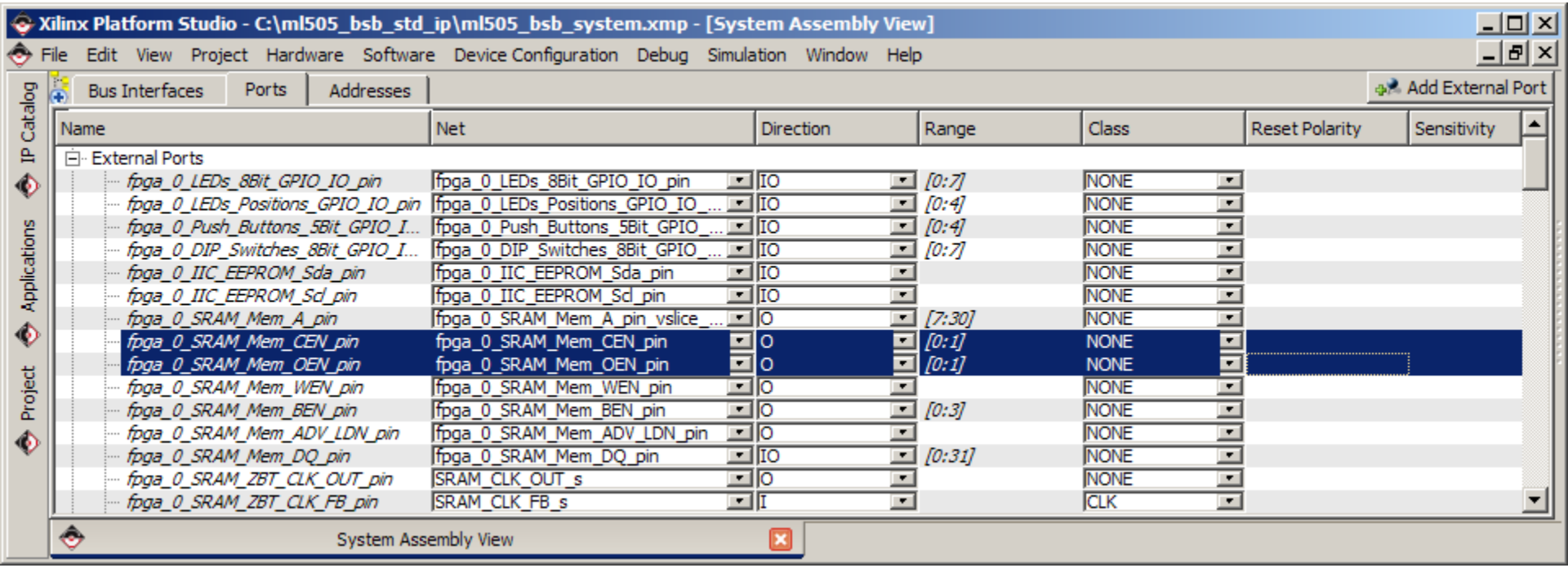
- **Expand this instance:**
  - **util_vector_logic_0**
  - Connect **Op1** to **sys_periph_reset**
  - Connect **Res** to **sys_periph_reset_n**



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

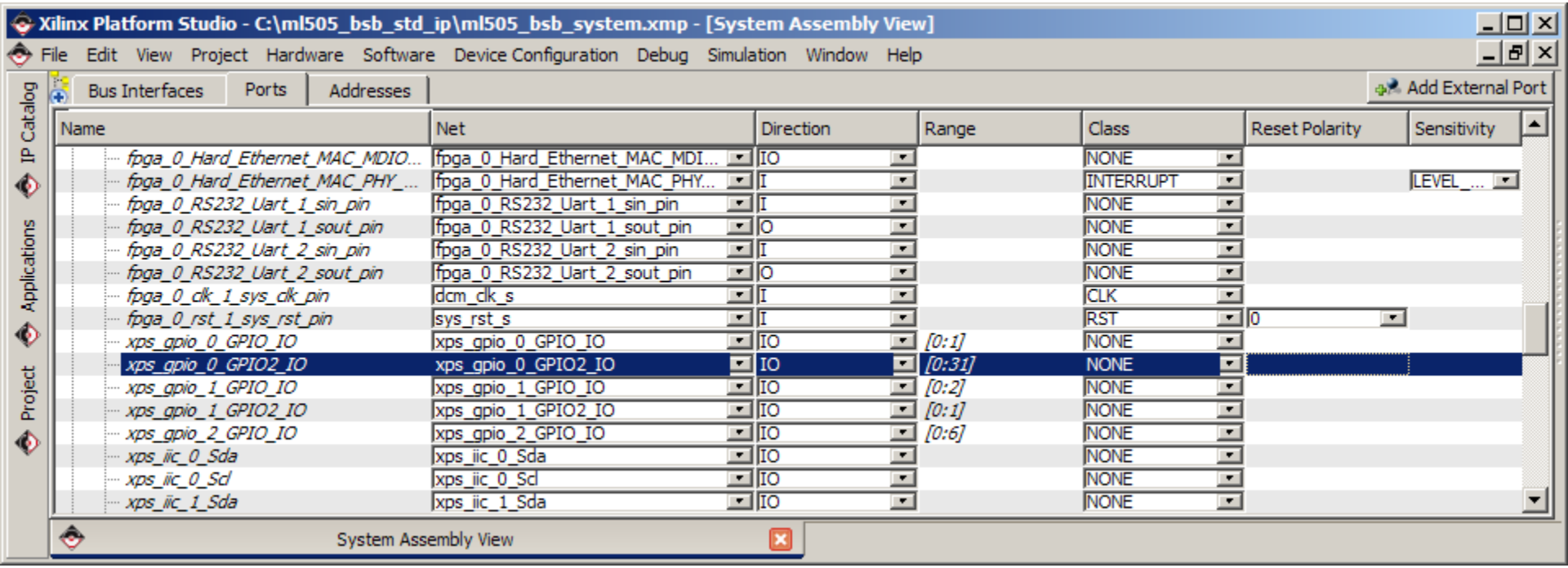
- **Expand External Ports**
  - Set **fpga_0_SRAM_Mem_CEN_pin** and **fpga_0_SRAM_Mem_OEN_pin** to a range of **[0:1]**



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

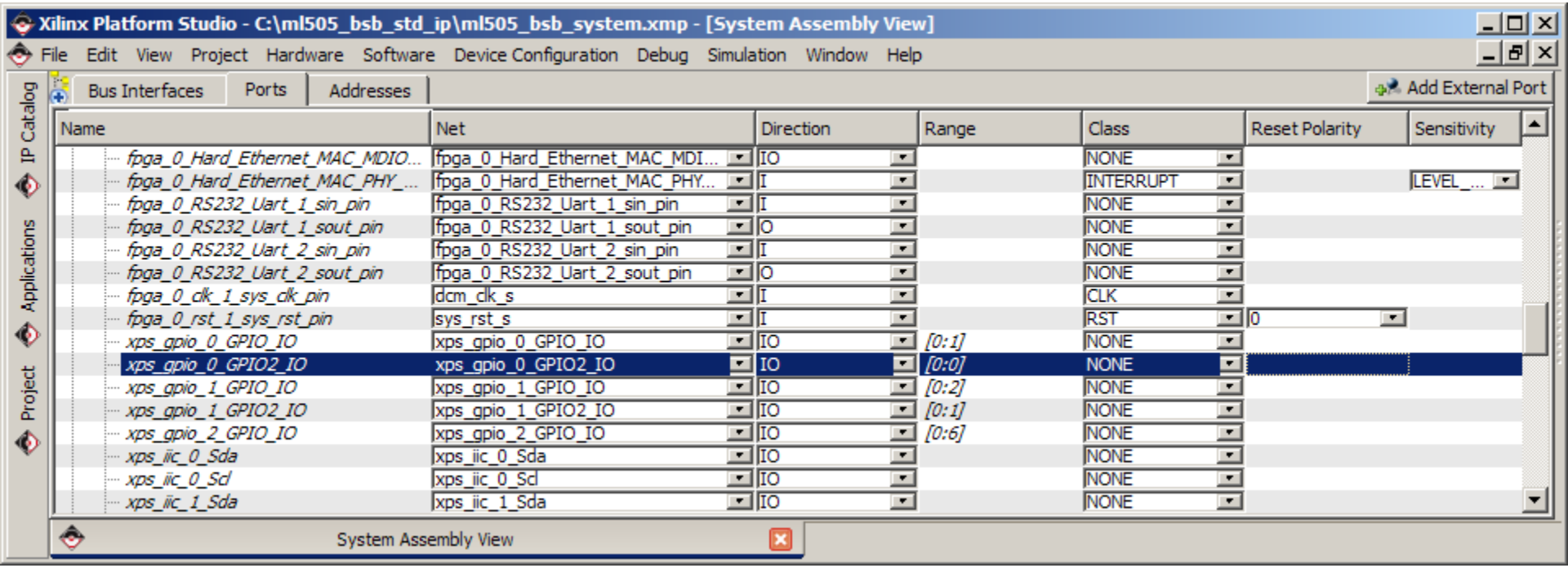
- **Apply AR35592**
  - The port, **xps_gpio_0_GPIO2_IO** is set to [0:31]
  - This needs to be a width of **[0:0]**



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

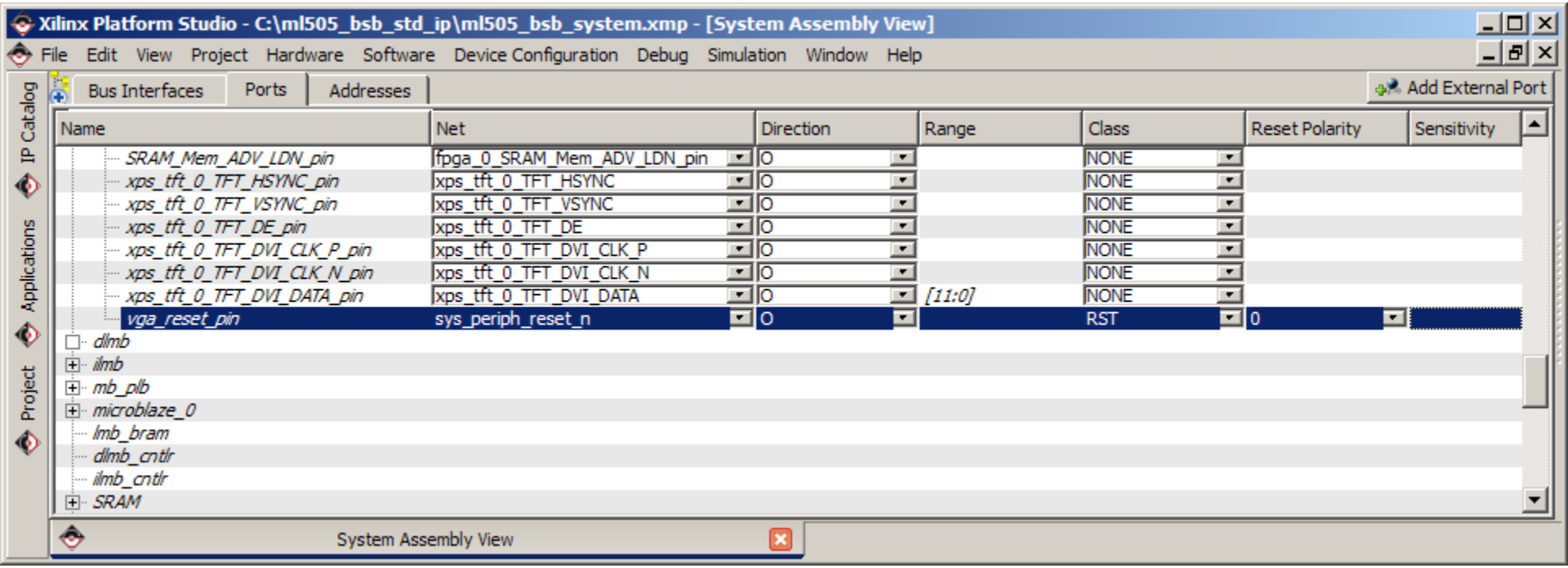
- Apply AR35592
  - Set **xps_gpio_0_GPIO2_IO** to a range of **[0:0]**



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

- **Add an External Port**
  - Click **Add External Port**
  - Pin name: **vga_reset_pin**
  - Net name: **sys_periph_reset_n**, Dir: **O**, Class: **RST**, Reset Polarity: **0**

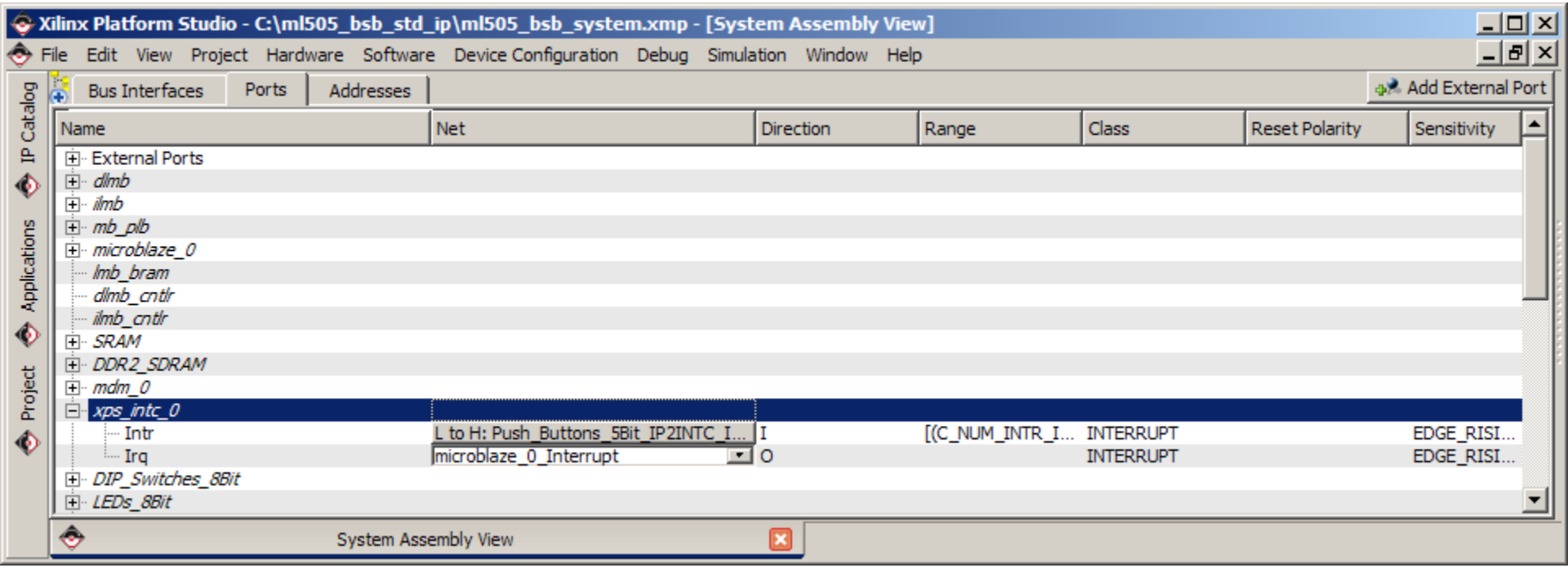


Note: Presentation applies to the ML505, ML506, and ML507

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Connect Ports

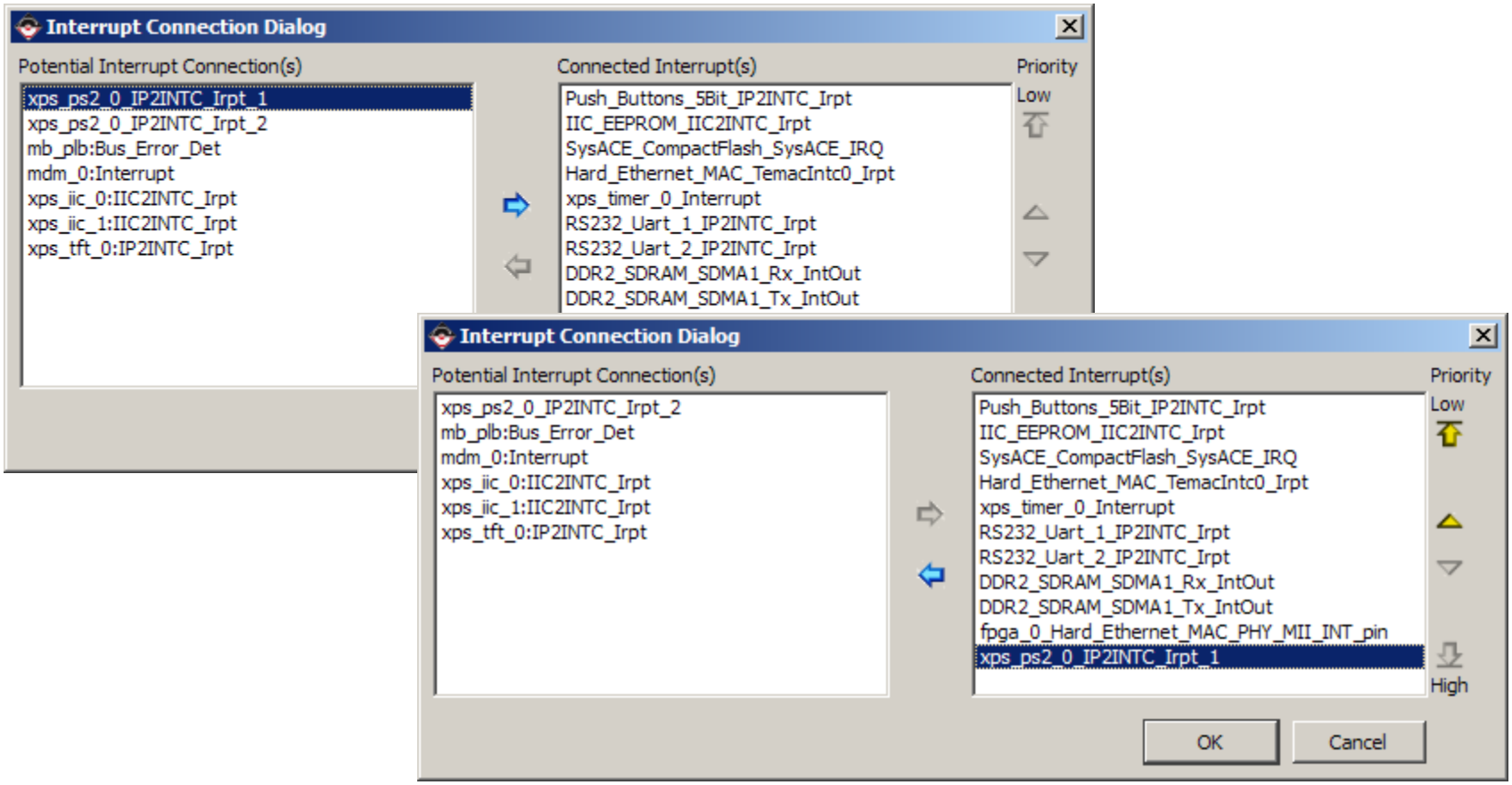
- **Expand this instance:**
  - **xps_intc_0**
  - Click on the gray Intr area to open the Interrupts dialog



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

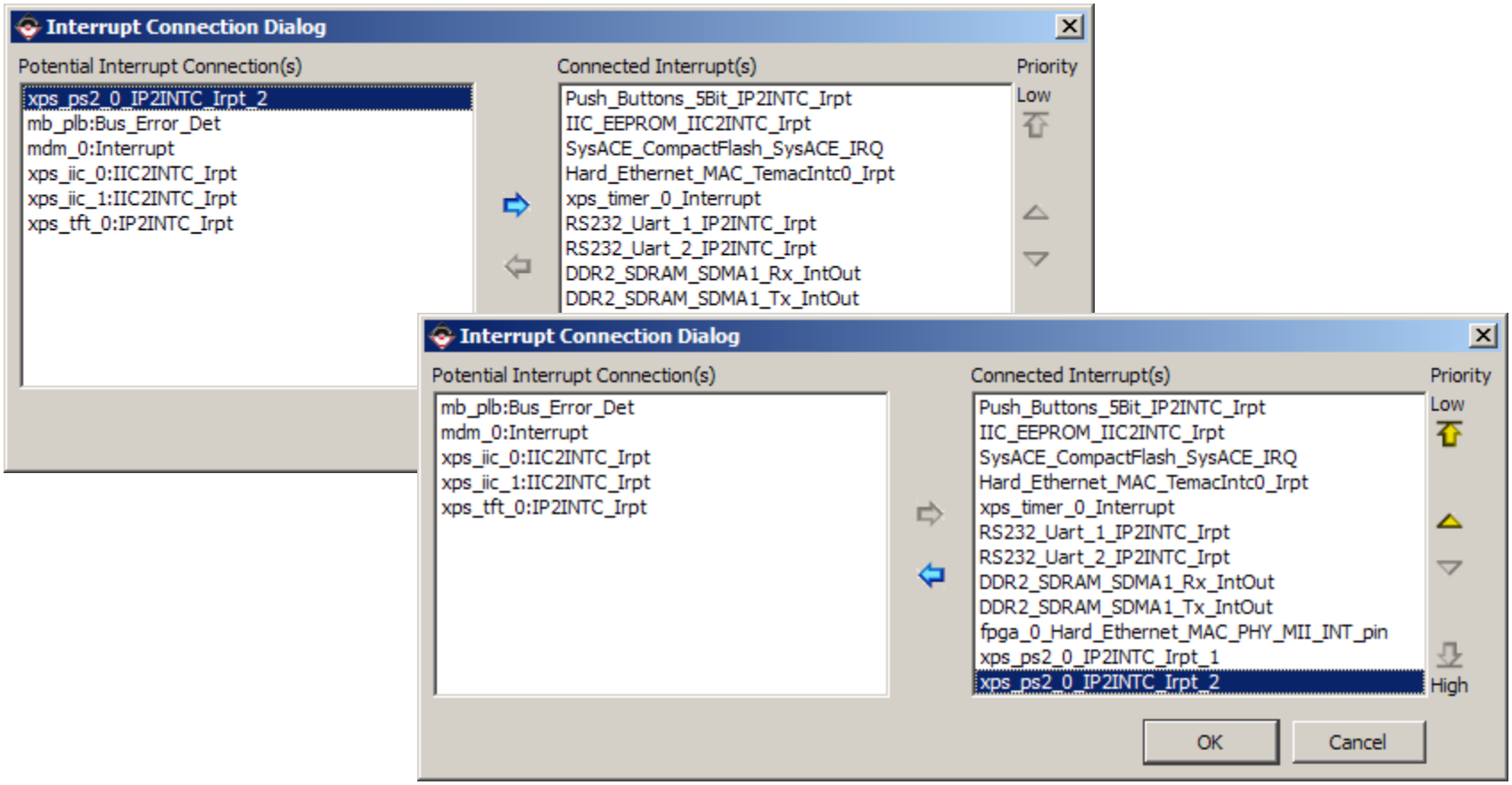
- **Add this interrupt:**
  - **xps_ps2_0_IP2INTC_Irpt_1**



Note: Presentation applies to the ML505, ML506, and ML507

Connect Ports

- **Add this interrupt:**
  - **xps_ps2_0_IP2INTC_Irpt_2**

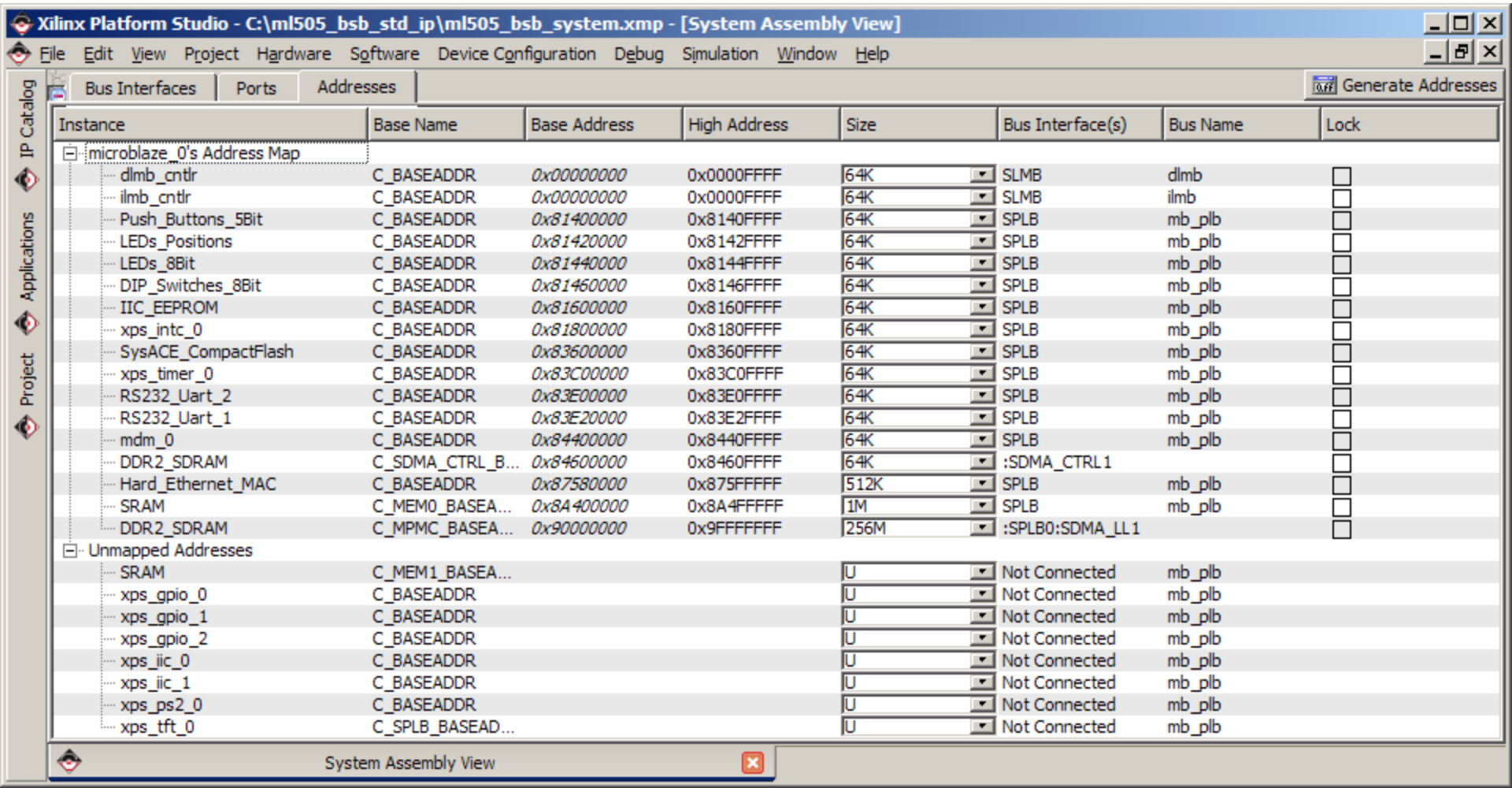


Note: Presentation applies to the ML505, ML506, and ML507

Generate Addresses

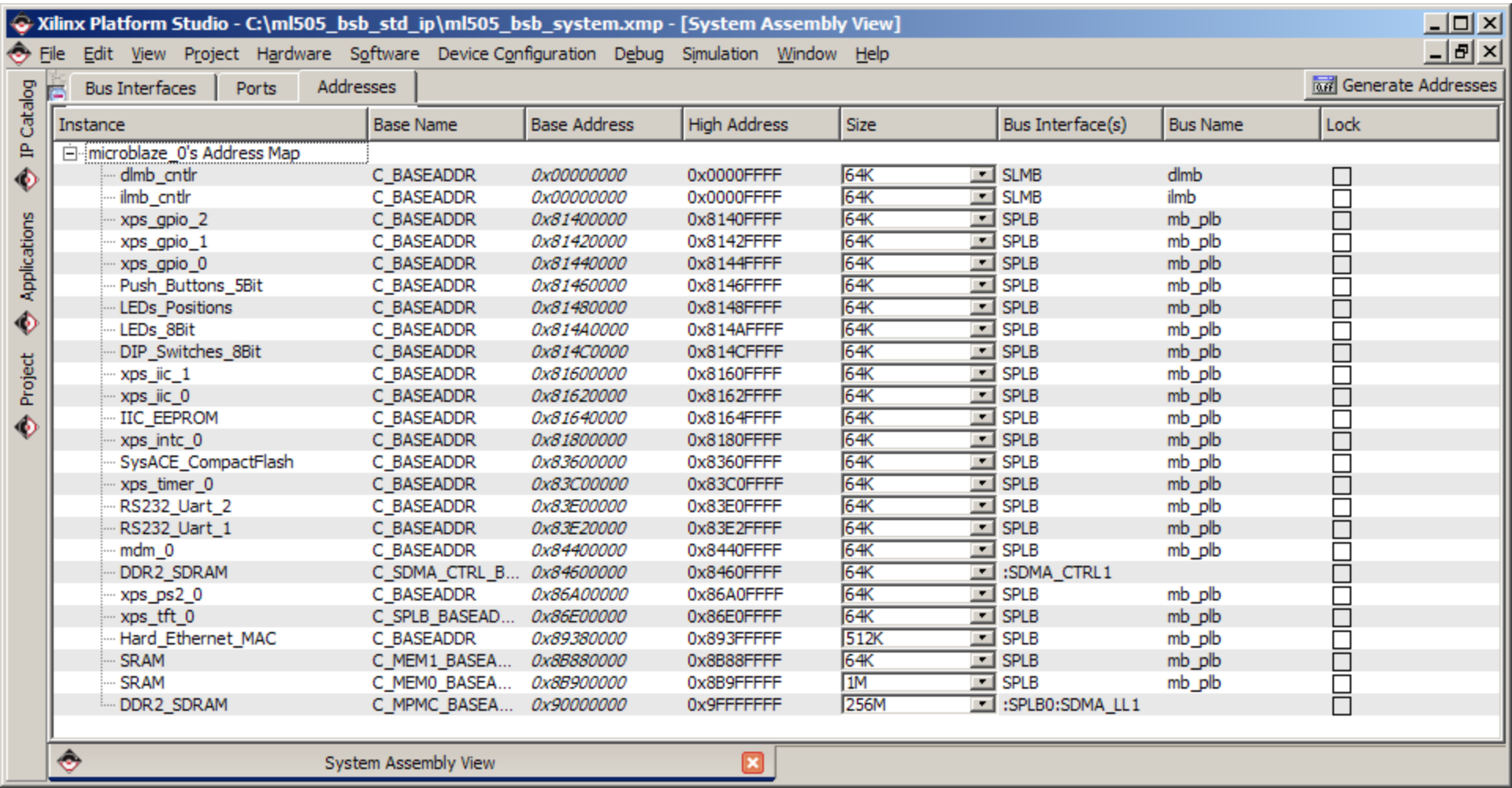
Generate Addresses

- **Select the Addresses tab**
  - Click the **Generate Addresses** Button



Generate Addresses

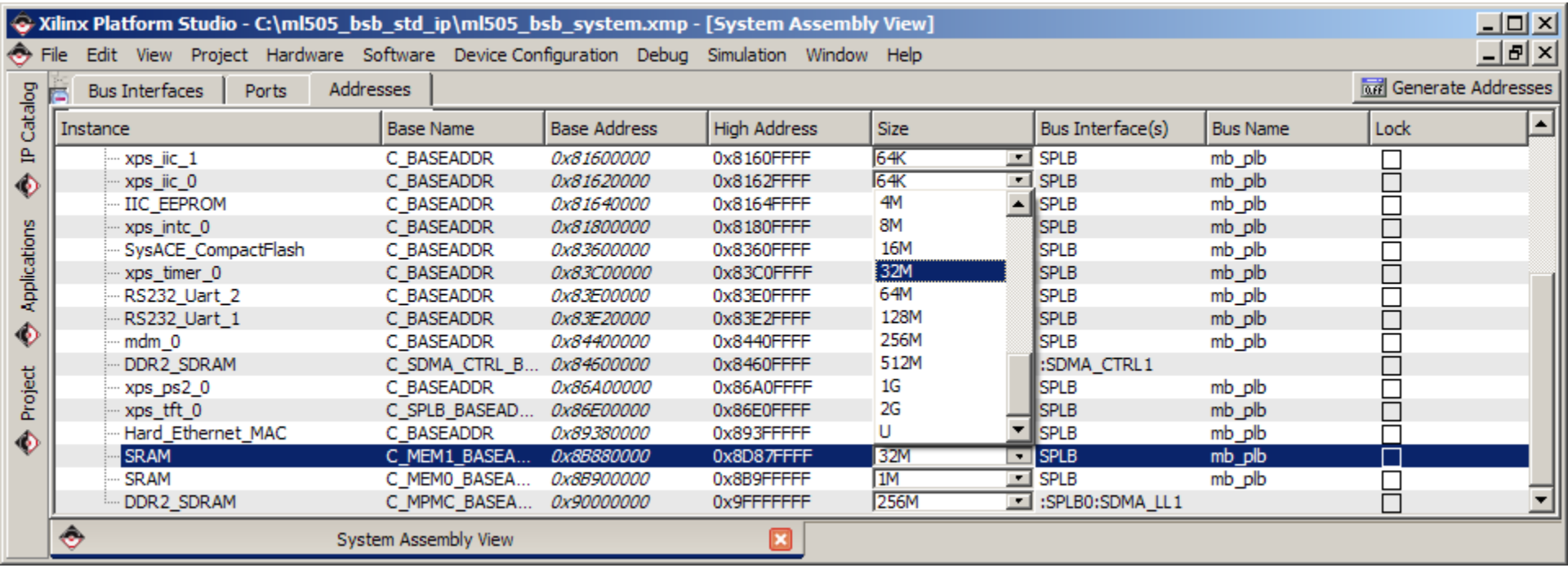
- The new addresses appear



Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
microblaze_0's Address Map							
dlmb_cntlr	C_BASEADDR	0x00000000	0x0000FFFF	64K	SLMB	dlmb	
ilmb_cntlr	C_BASEADDR	0x00000000	0x0000FFFF	64K	SLMB	ilmb	
xps_gpio_2	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	mb_plb	
xps_gpio_1	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	mb_plb	
xps_gpio_0	C_BASEADDR	0x81440000	0x8144FFFF	64K	SPLB	mb_plb	
Push_Buttons_5Bit	C_BASEADDR	0x81460000	0x8146FFFF	64K	SPLB	mb_plb	
LEDs_Positions	C_BASEADDR	0x81480000	0x8148FFFF	64K	SPLB	mb_plb	
LEDs_8Bit	C_BASEADDR	0x814A0000	0x814AFFFF	64K	SPLB	mb_plb	
DIP_Switches_8Bit	C_BASEADDR	0x814C0000	0x814CFFFF	64K	SPLB	mb_plb	
xps_iic_1	C_BASEADDR	0x81600000	0x8160FFFF	64K	SPLB	mb_plb	
xps_iic_0	C_BASEADDR	0x81620000	0x8162FFFF	64K	SPLB	mb_plb	
IIC_EEPROM	C_BASEADDR	0x81640000	0x8164FFFF	64K	SPLB	mb_plb	
xps_intc_0	C_BASEADDR	0x81800000	0x8180FFFF	64K	SPLB	mb_plb	
SysACE_CompactFlash	C_BASEADDR	0x83600000	0x8360FFFF	64K	SPLB	mb_plb	
xps_timer_0	C_BASEADDR	0x83C00000	0x83C0FFFF	64K	SPLB	mb_plb	
RS232_Uart_2	C_BASEADDR	0x83E00000	0x83E0FFFF	64K	SPLB	mb_plb	
RS232_Uart_1	C_BASEADDR	0x83E20000	0x83E2FFFF	64K	SPLB	mb_plb	
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	SPLB	mb_plb	
DDR2_SDRAM	C_SDMA_CTRL_B...	0x84600000	0x8460FFFF	64K	:SDMA_CTRL1		
xps_ps2_0	C_BASEADDR	0x86A00000	0x86A0FFFF	64K	SPLB	mb_plb	
xps_tft_0	C_SPLB_BASEAD...	0x86E00000	0x86E0FFFF	64K	SPLB	mb_plb	
Hard_Ethernet_MAC	C_BASEADDR	0x89380000	0x893FFFFF	512K	SPLB	mb_plb	
SRAM	C_MEM1_BASEA...	0x8B880000	0x8B88FFFF	64K	SPLB	mb_plb	
SRAM	C_MEM0_BASEA...	0x8B900000	0x8B9FFFFF	1M	SPLB	mb_plb	
DDR2_SDRAM	C_MPMC_BASEA...	0x90000000	0x9FFFFFFF	256M	:SPLB0:SDMA_LL1		

Generate Addresses

- **The Flash is 32 Megabytes**
  - Set C_MEM1_BASEADDR to 32M
  - Click the **Generate Addresses** Button again

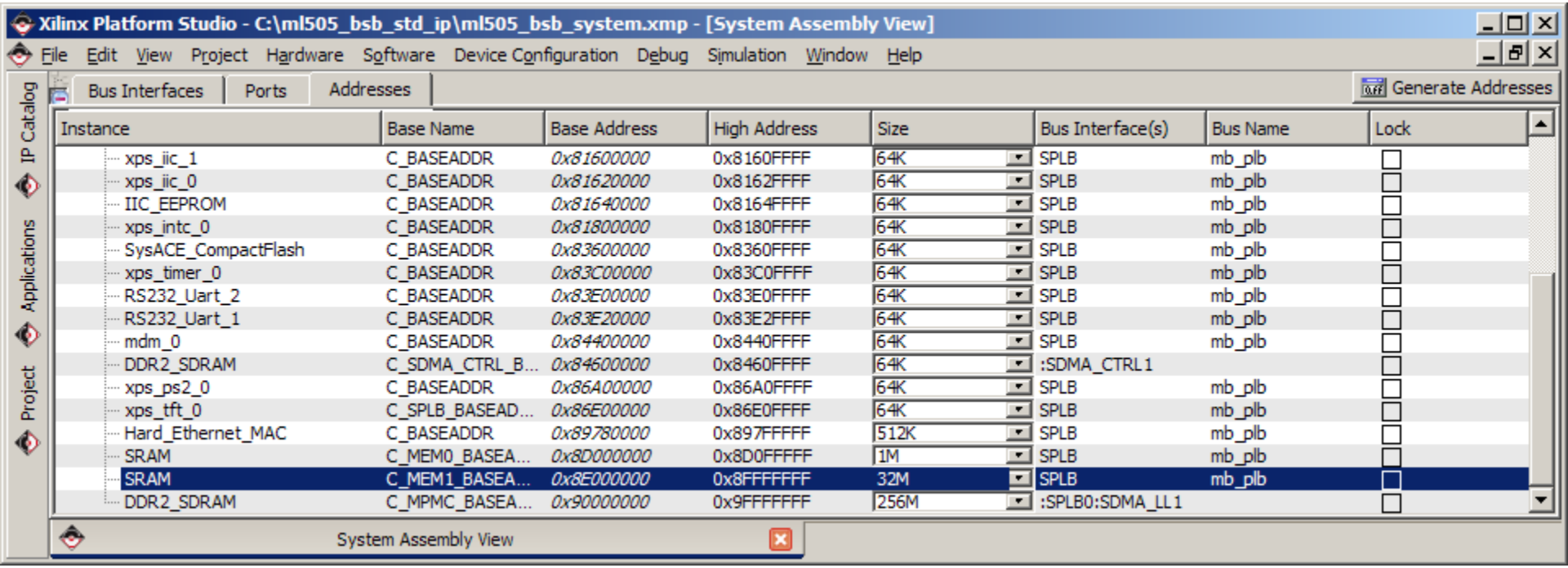


Note: Presentation applies to the ML505, ML506, and ML507

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Generate Addresses

- **The new addresses appear**
  - The FLASH now has a full 32M address range



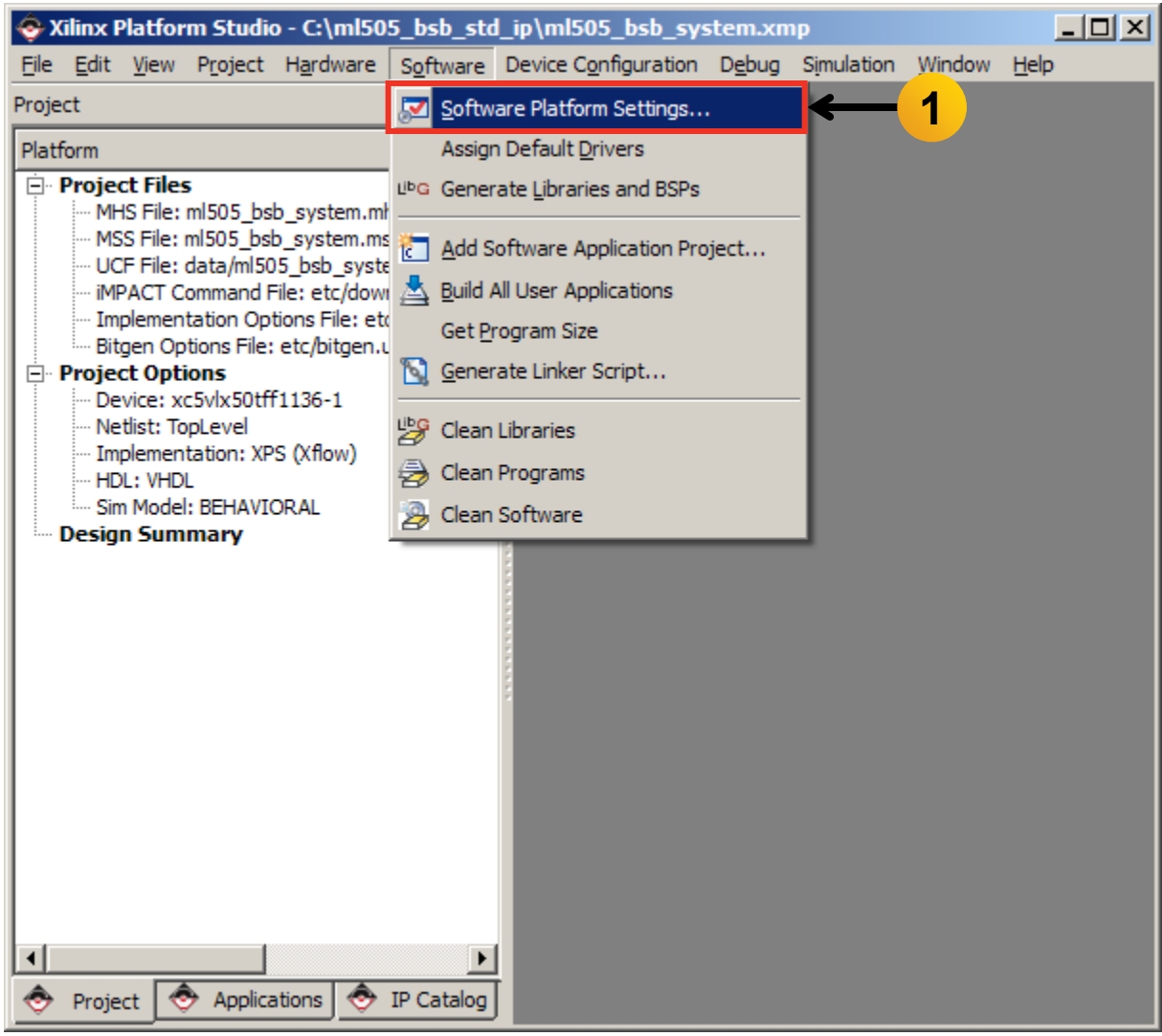
Note: Presentation applies to the ML505, ML506, and ML507

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Software Configuration

Software Platform Settings

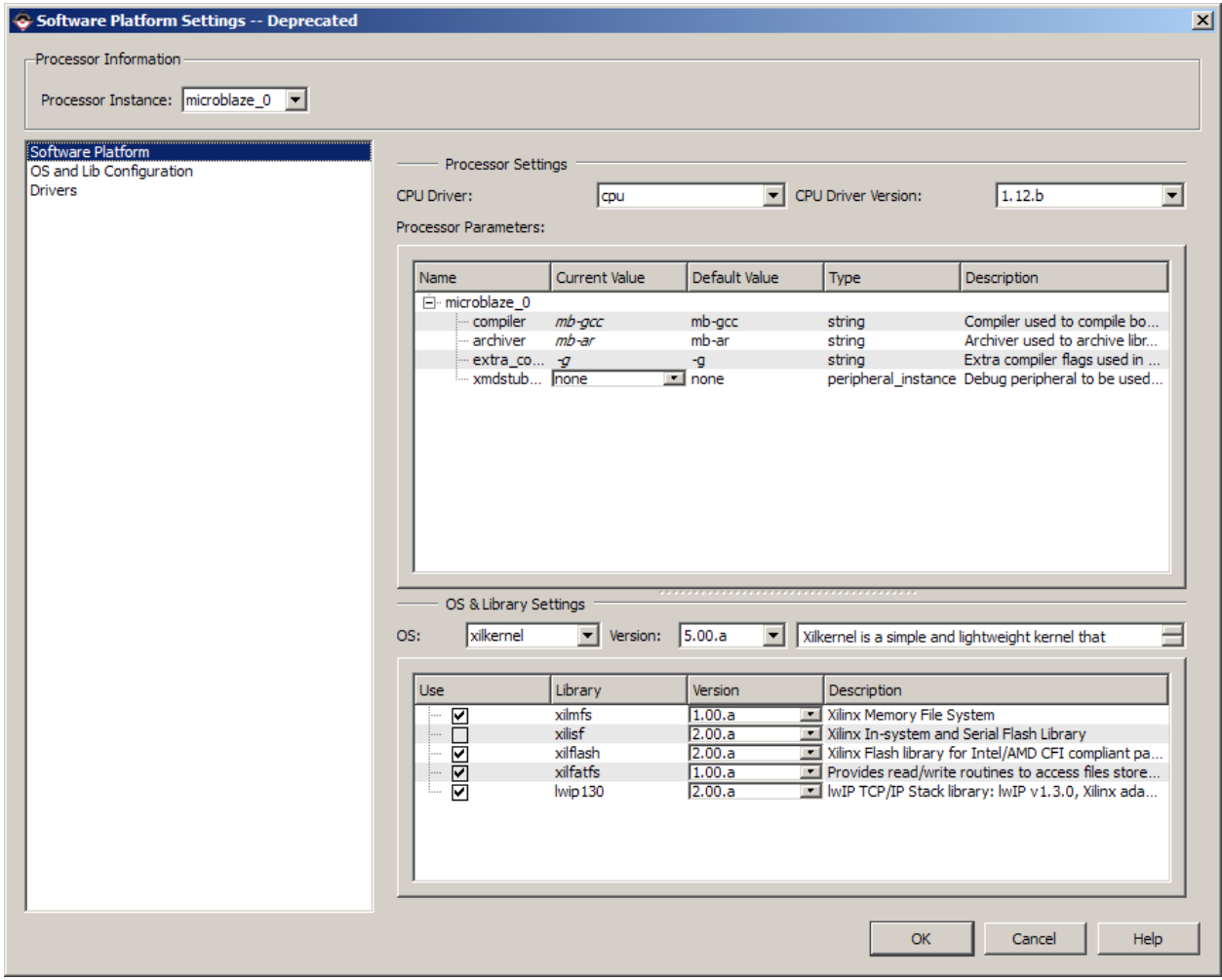
- **Configure the Software Platform**
  - Select **Software → Software Platform Settings…** (1)



Note: Presentation applies to the ML505, ML506, and ML507

Software Platform Settings

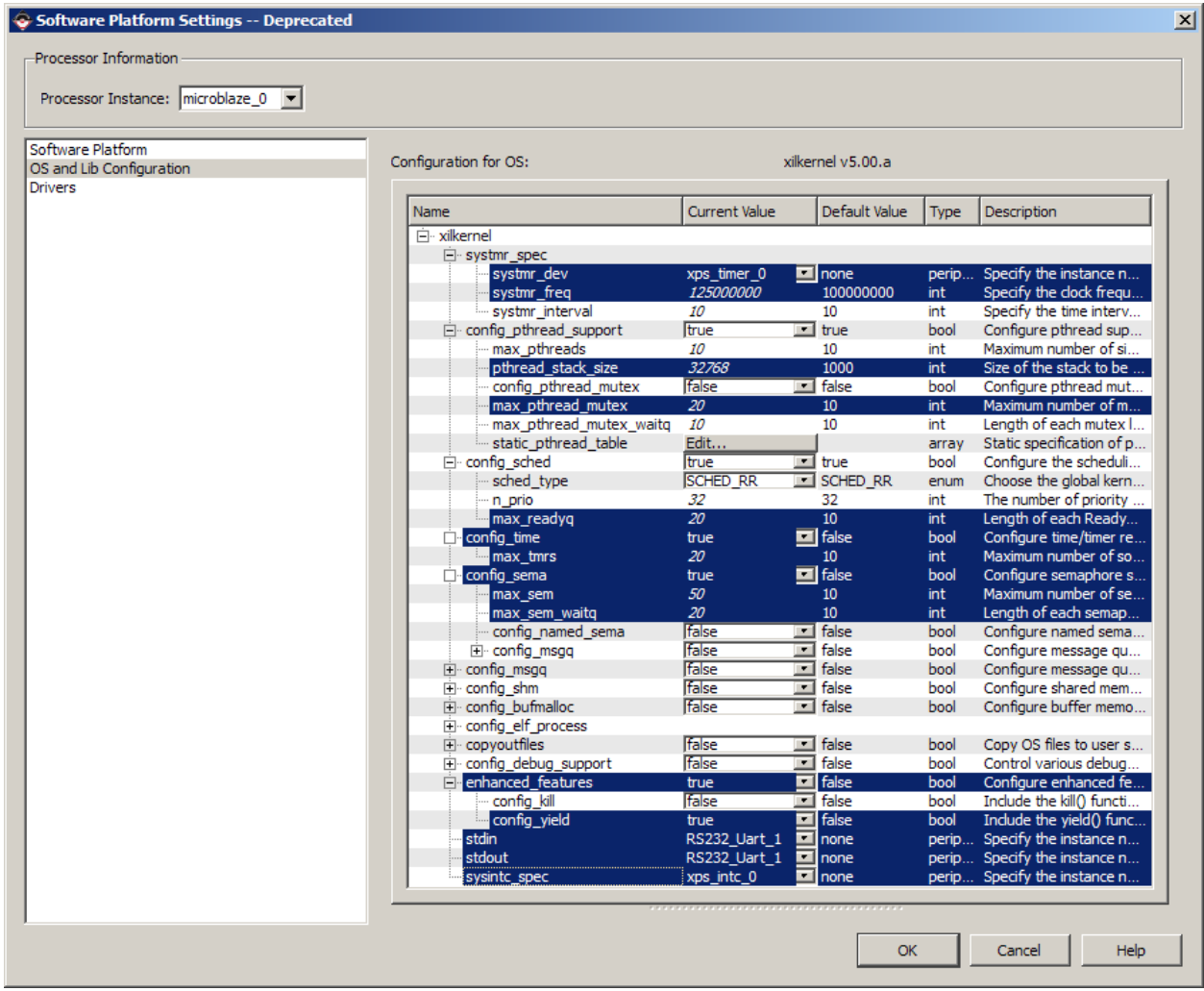
- **Under Software Platform**
  - Set OS to **xilkernel**
  - Select **xilmfs**, **xilflash**, **xilfatfs**, and **lwip130**



Note: Presentation applies to the ML505, ML506, and ML507

Software Platform Settings

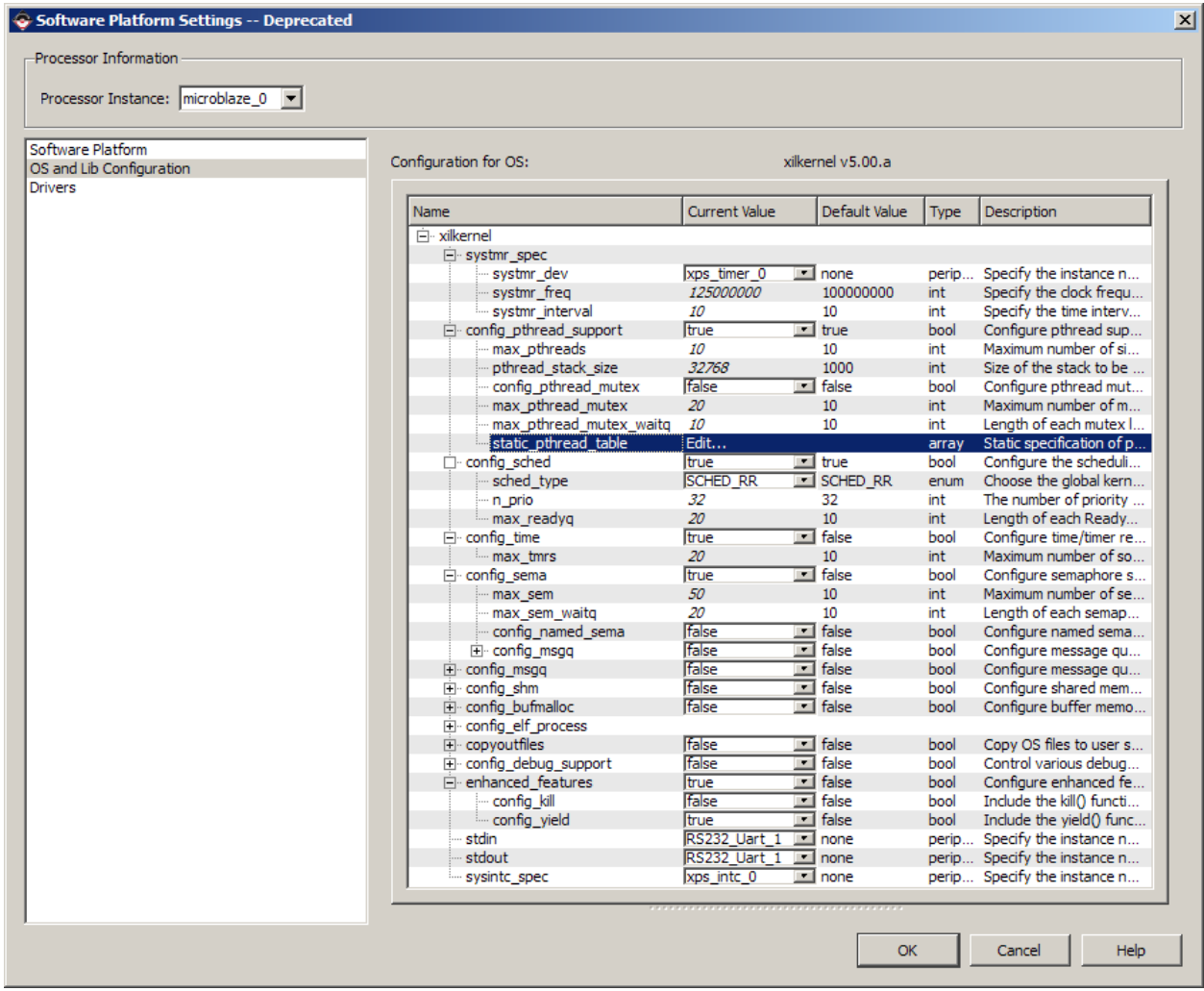
- **Under OS and Libraries, Configuration for OS, set these xilkernel settings:**
  - systmr_dev = **xps_timer_0**
  - systmr_freq = **125000000**
  - pthread_stack_size = **32768**
  - max_pthread_mutex = **20**
  - max_readyq = **20**
  - config_time = **true**
  - max_tmrs = **20**
  - config_sema = **true**
  - max_sem = **50**
  - max_sem_waitq = **20**
  - enhanced_features = **true**
  - config_yield = **true**
  - stdin = **RS232_Uart_1**
  - stdout = **RS232_Uart_1**
  - sysintc_spec = **xps_intc_0**



Note: Presentation applies to the ML505, ML506, and ML507

Software Platform Settings

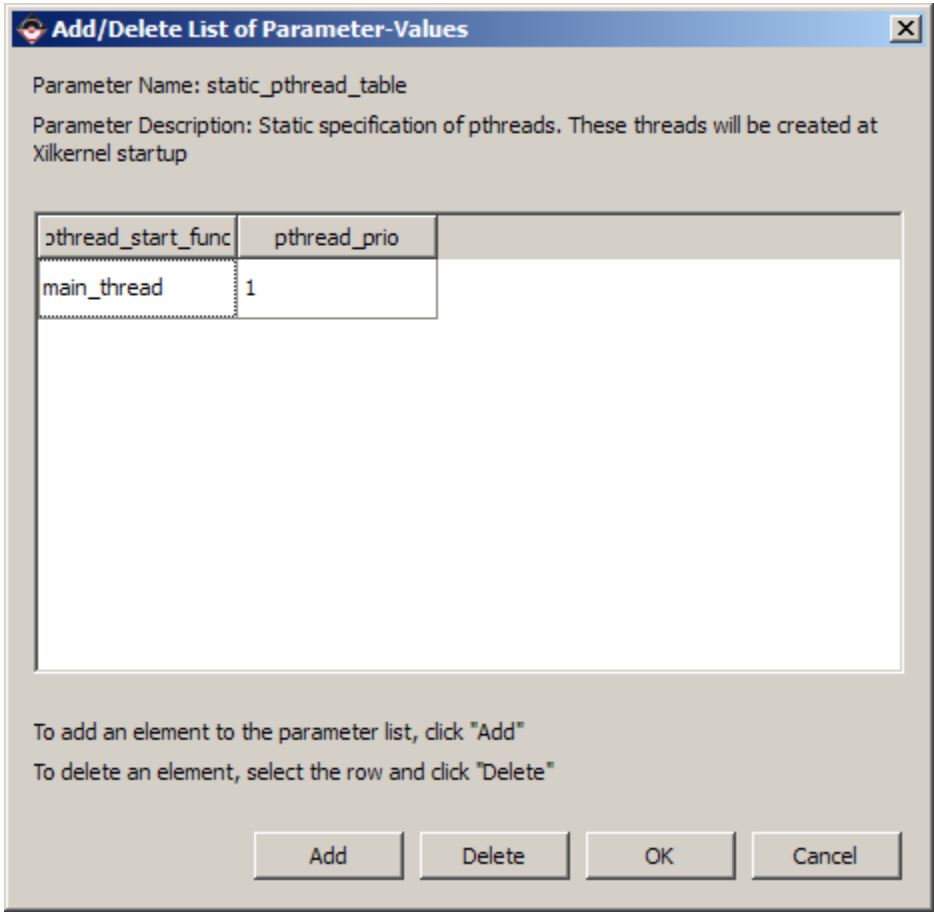
- **Under OS and Libraries, Configuration for OS**
  - Click static_pthread_table



Note: Presentation applies to the ML505, ML506, and ML507

Software Platform Settings

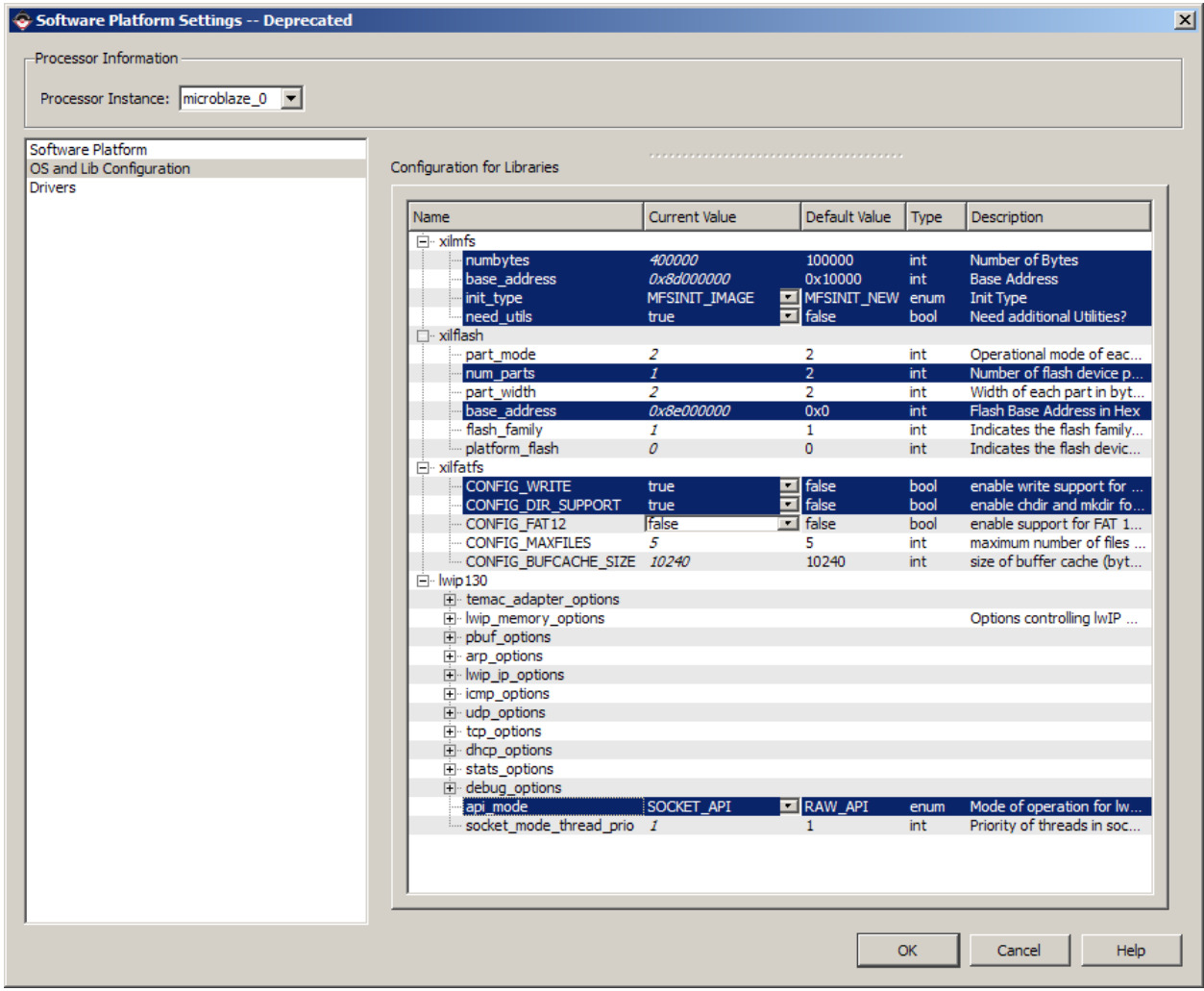
- **Edit the static_pthread_table**
  - Click Add
  - Set **pthread_start_func = main_thread**
  - Set **pthread_prio = 1**



Note: Presentation applies to the ML505, ML506, and ML507

Software Platform Settings

- **Under OS and Libraries, Configuration for Libraries, make these settings**
  - numbytes = **400000**
  - base_address = **0x8d000000**
    - **sram flash address**
  - int_type to **MFSINIT_IMAGE**
  - need_utils = **true**
  - num_parts: 1
  - base_address = **0x8e000000**
    - sram address
  - CONFIG_WRITE = **true**
  - CONFIG_DIR_SUPPORT = **true**
  - api_mode = **SOCKET_API**

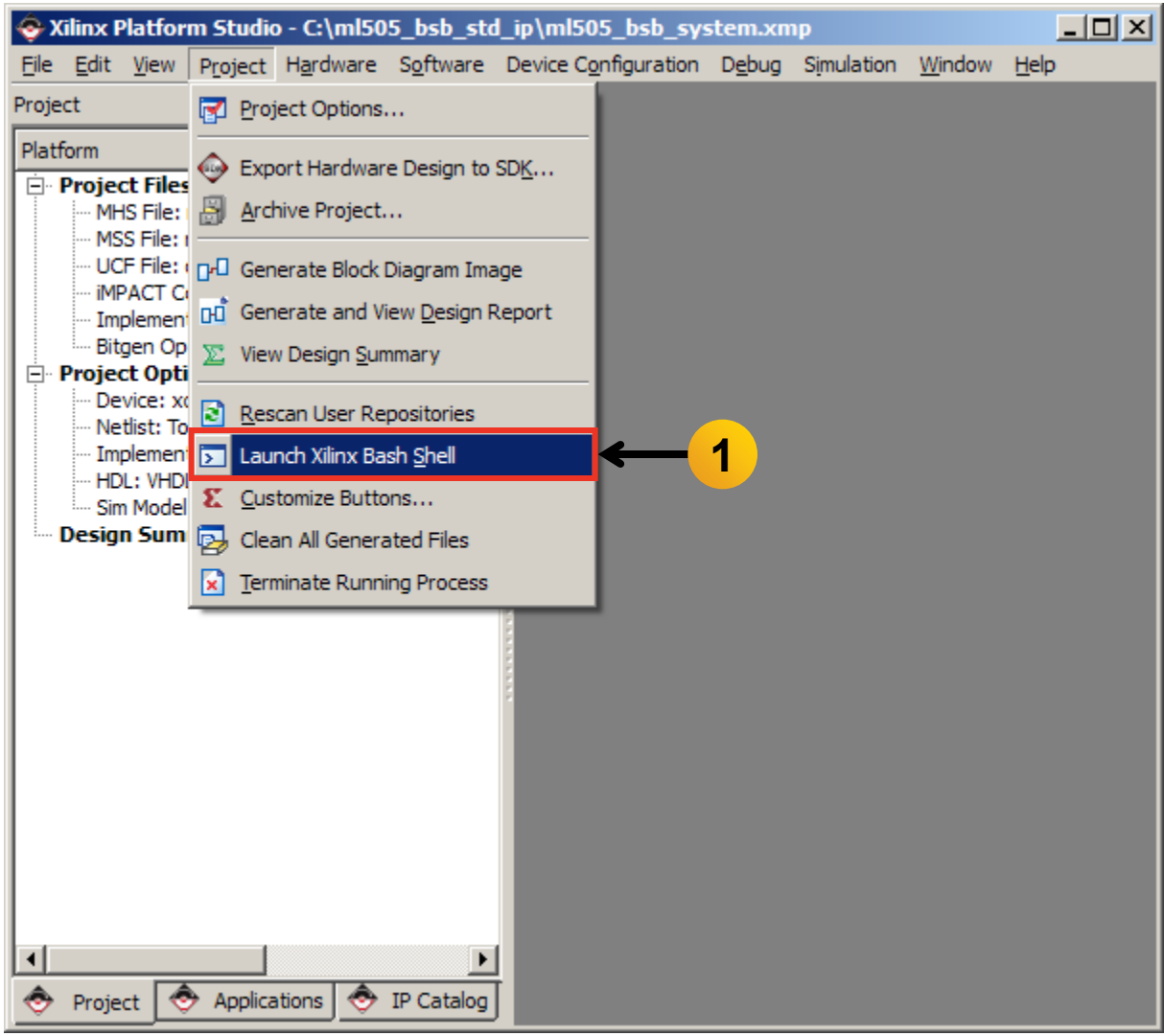


Note: Presentation applies to the ML505, ML506, and ML507

Create MFS Image

Create MFS Image

- **Open an EDK shell**
  - Select **Project** → **Launch EDK Shell** (1)



Note: Presentation applies to the ML505, ML506, and ML507

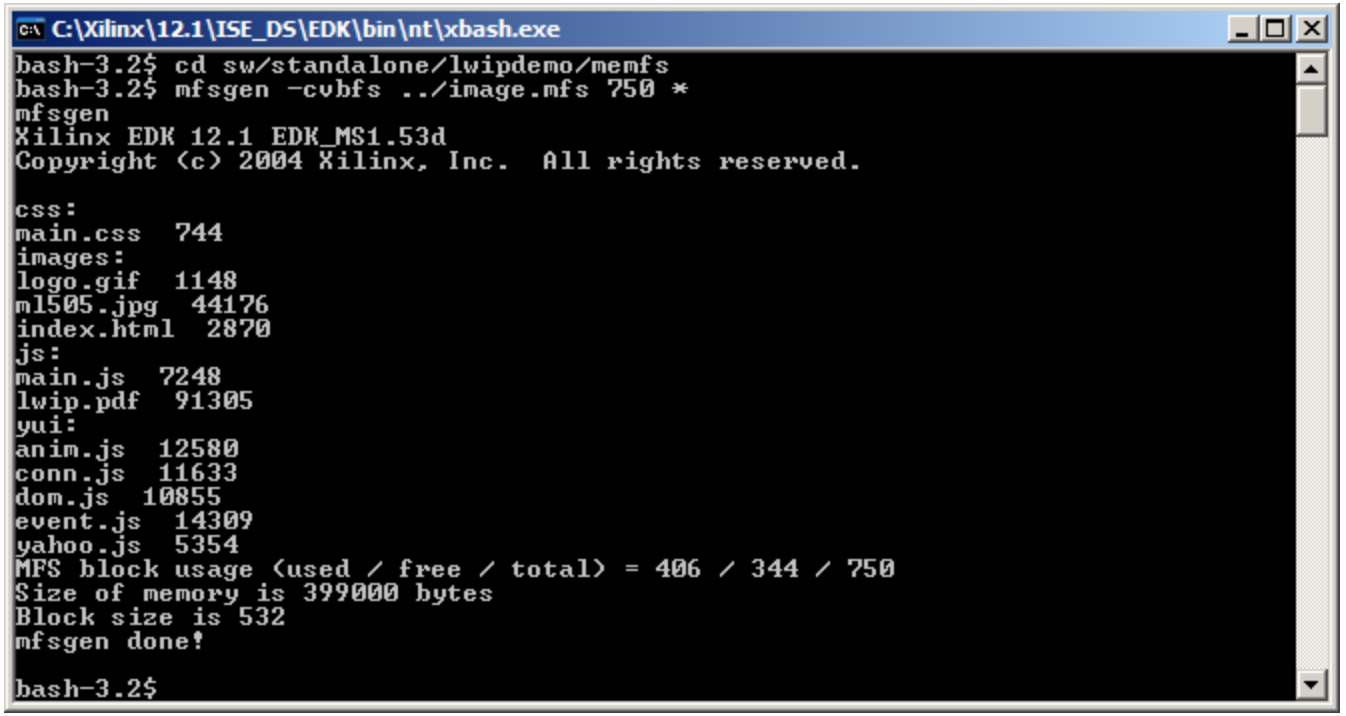
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Create MFS Image

- At the bash prompt, type (1):

  cd sw/standalone/lwipdemo/memfs

  mfsgen -cvbfs ../image.mfs 750 *

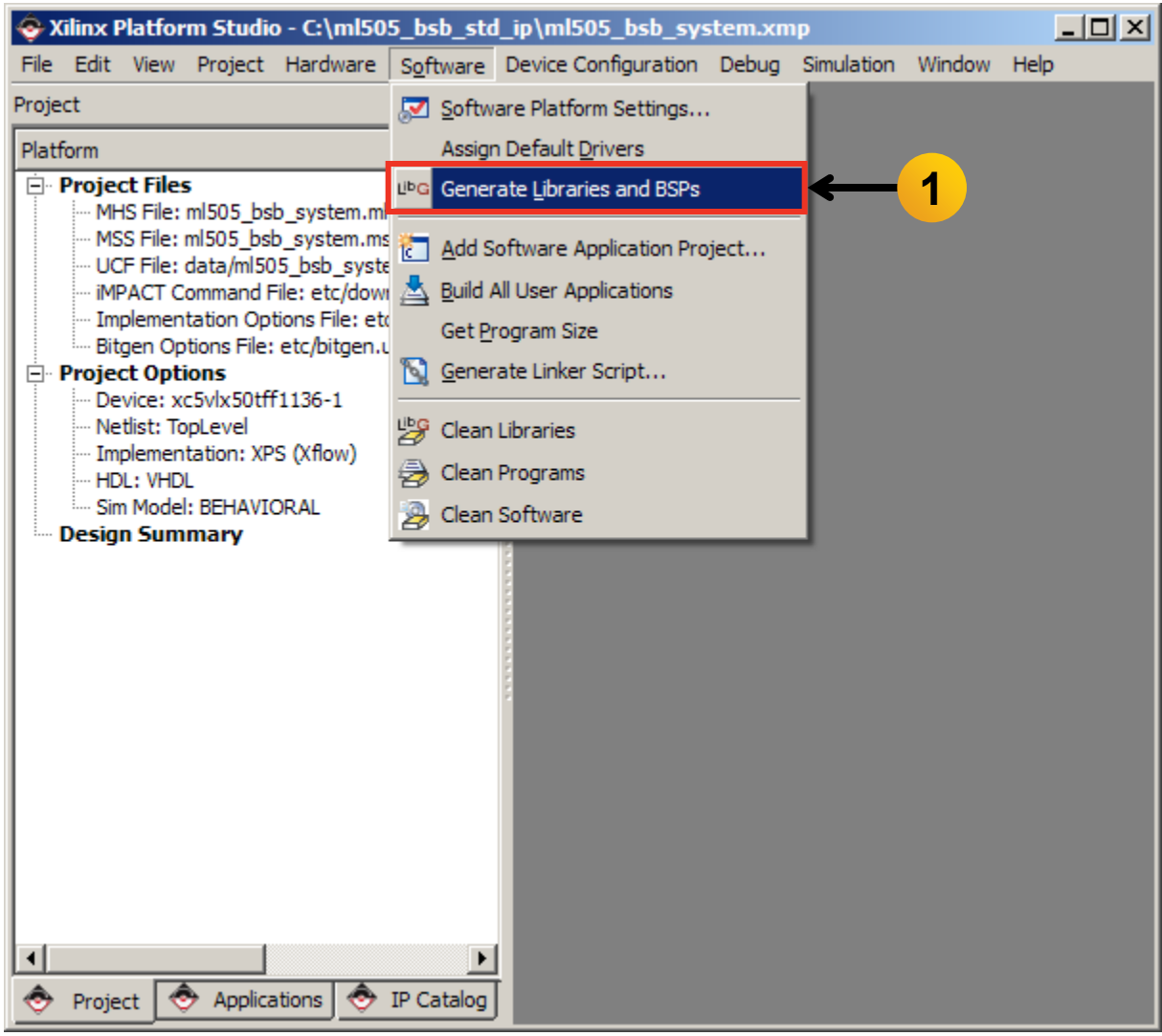


Note: Presentation applies to the ML505, ML506, and ML507

Compile Standard IP Design

Generate the ELF Files

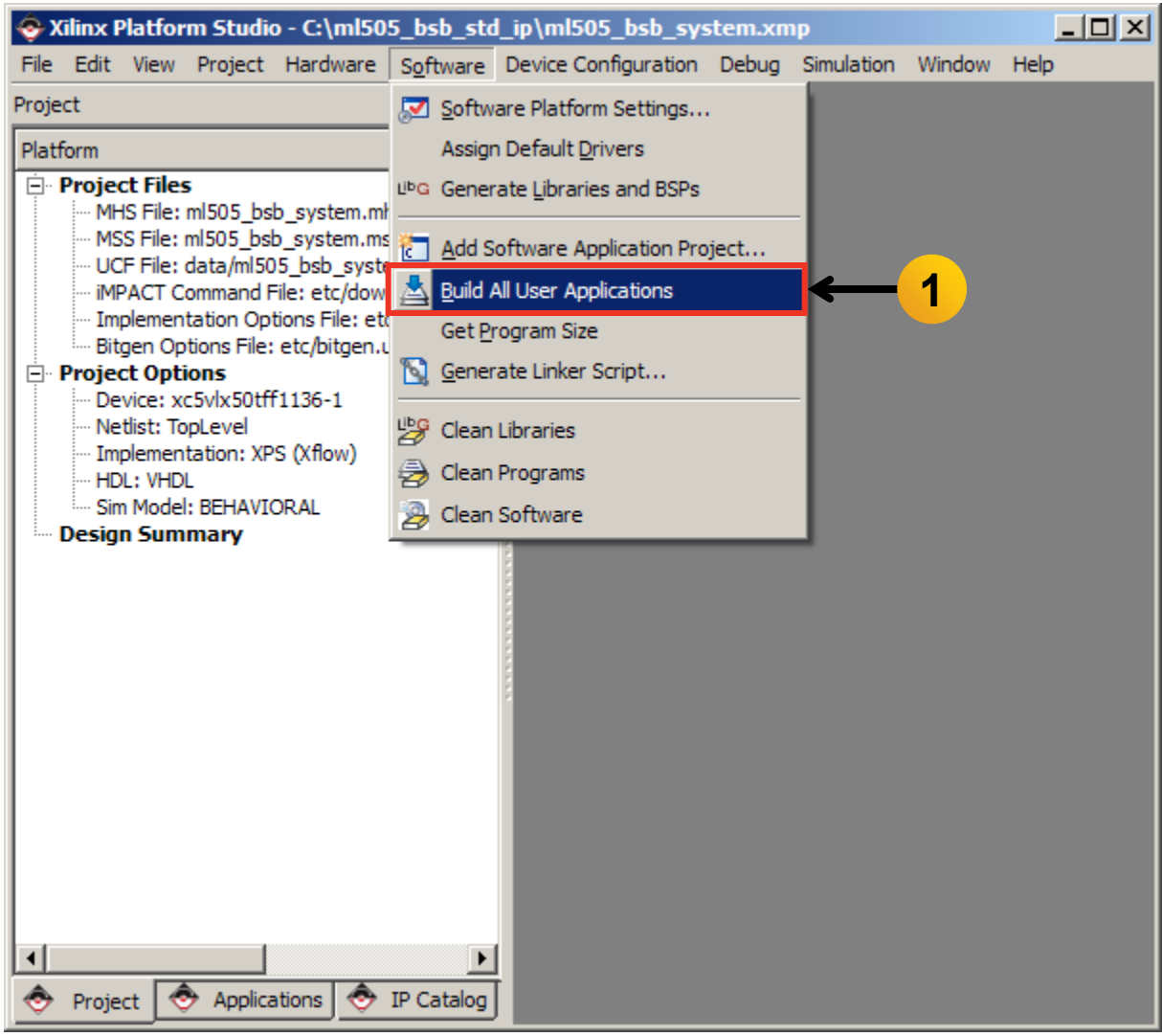
- **Generate the libraries needed to create the bitstream**
  - Select **Software → Generate Libraries and BSPs** (1)



Note: Presentation applies to the ML505, ML506, and ML507

Generate the ELF Files

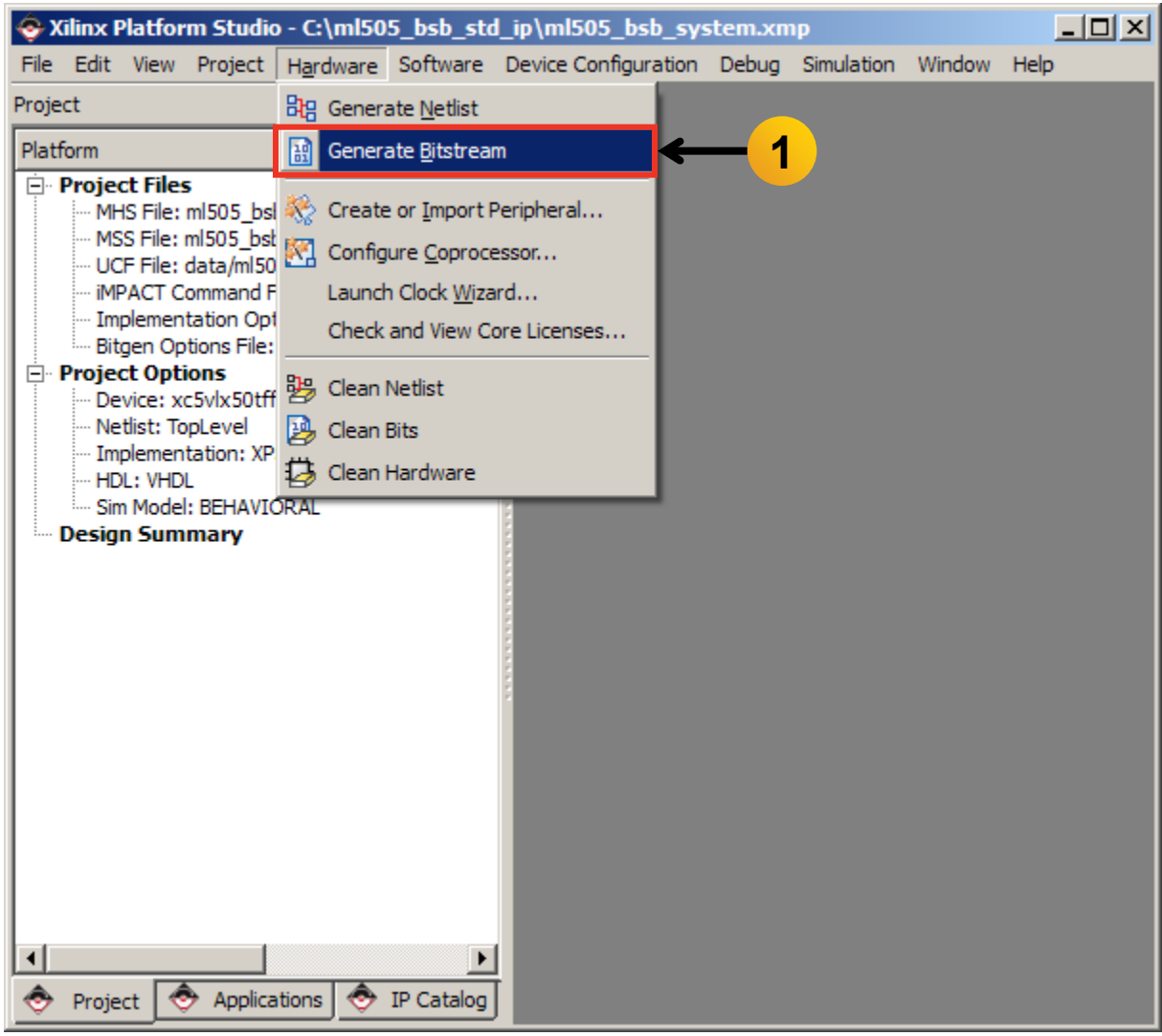
- **Compile the Software Applications and create an executable (executable.elf)**
  - Select **Software → Build All User Applications** (1)



Note: Presentation applies to the ML505, ML506, and ML507

Generate the Bitstream

- **Create the hardware design, ml505_bsb_system.bit that is located in <project directory> /implementation**
  - Select **Hardware → Generate Bitstream** (1)



Note: Presentation applies to the ML505, ML506, and ML507

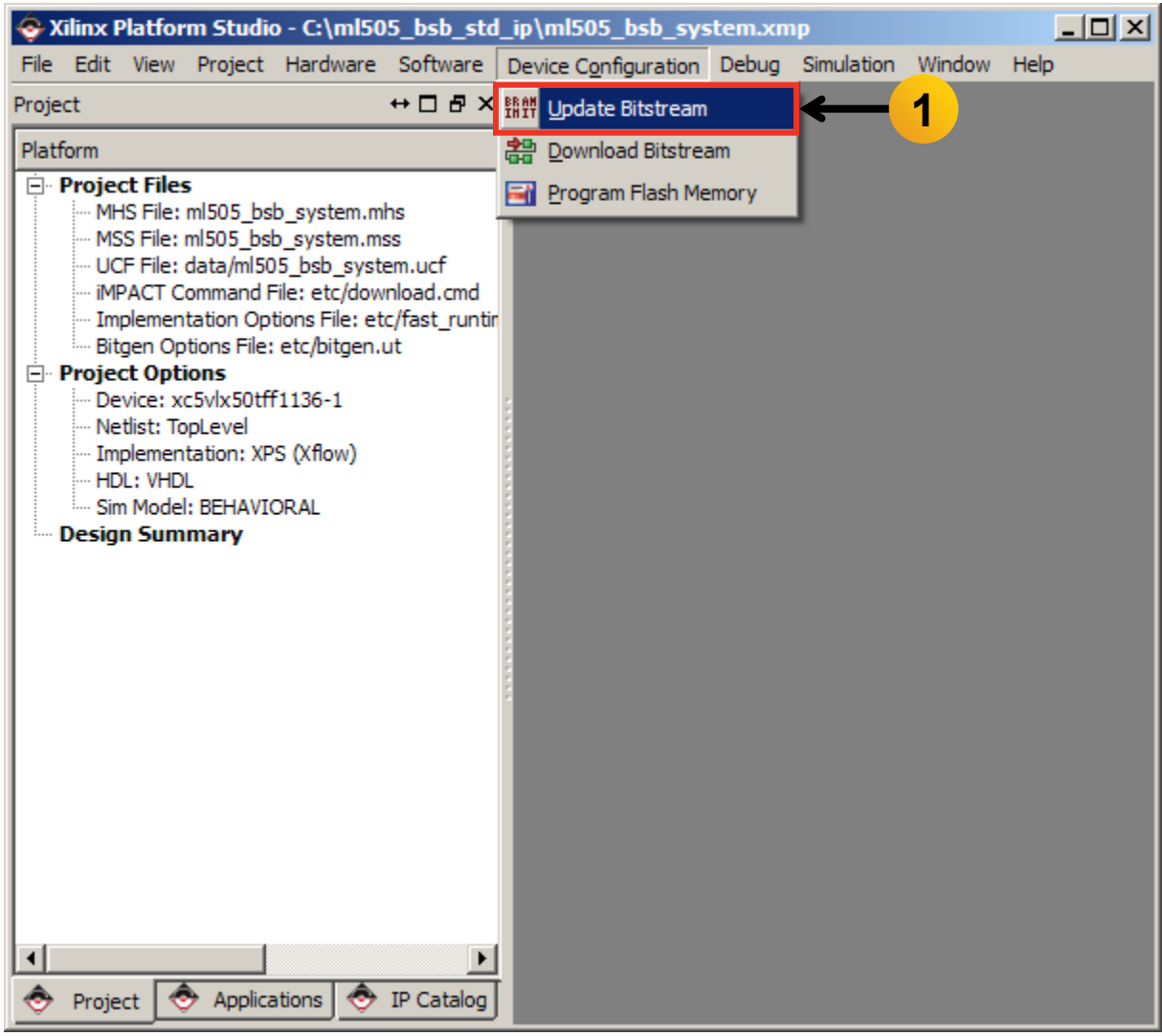
Loading a Bootloop ELF into the Block RAM

- A concatenated software/hardware file, known as an ACE file, is useful for loading large programs, such as a Linux, VxWorks, or U-Boot into the external memory
- A bootloop program must be used to occupy the processor until the software is loaded into memory
- The following pages show how to initialize a bootloop program into Block RAM and to test its existence

Note: Presentation applies to the ML505, ML506, and ML507

Loading a Bootloop ELF into the Block RAM

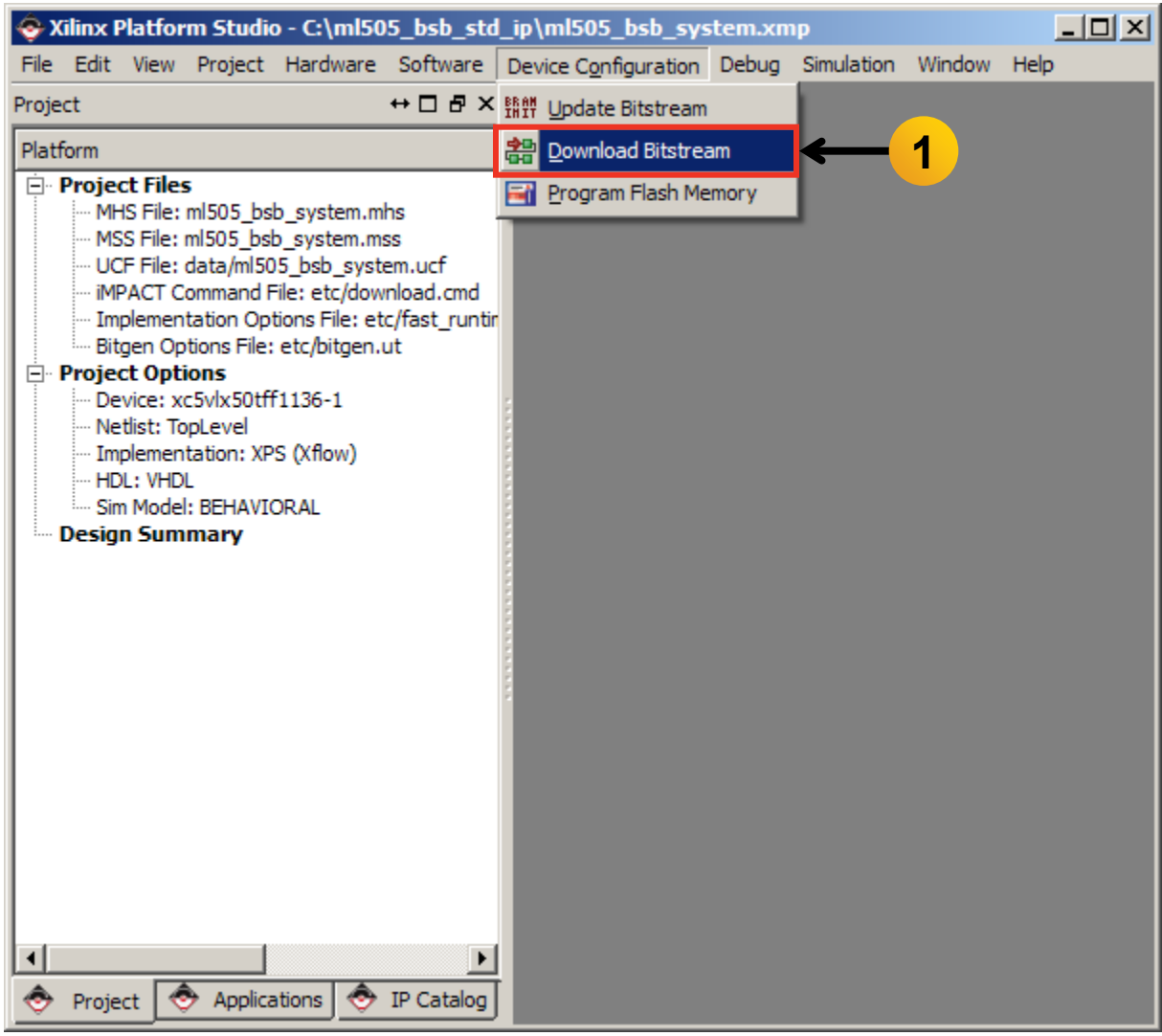
- **Update the bitstream (download.bit) with a bootloop ELF file (microblaze_0.elf)**
  - Select **Device Configuration → Update Bitstream** (1)



Note: Presentation applies to the ML505, ML506, and ML507

Loading a Bootloop ELF into the Block RAM

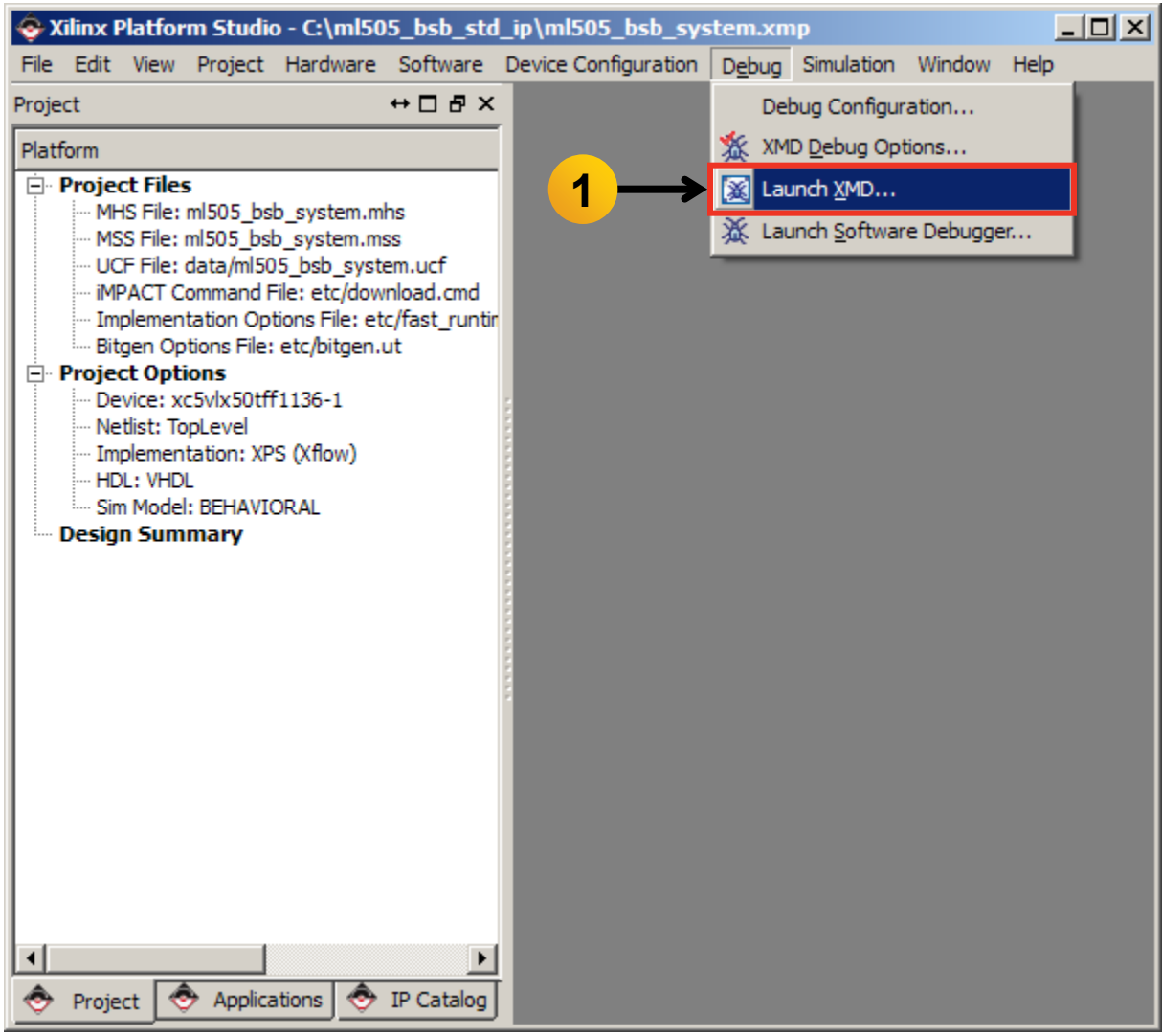
- **Load the new design onto the FPGA and load the bootloop program into the Block RAM**
  - Select **Device Configuration → Download Bitstream** (1)



Note: Presentation applies to the ML505, ML506, and ML507

Loading a Bootloop ELF into the Block RAM

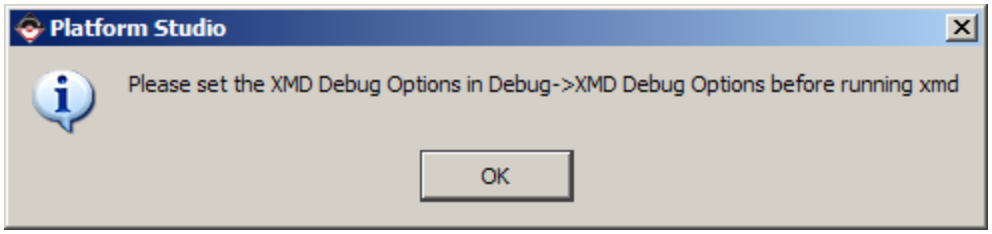
- **A memory read can be executed to test if bootloop was successfully loaded**
  - Select **Debug → Launch XMD** (1)

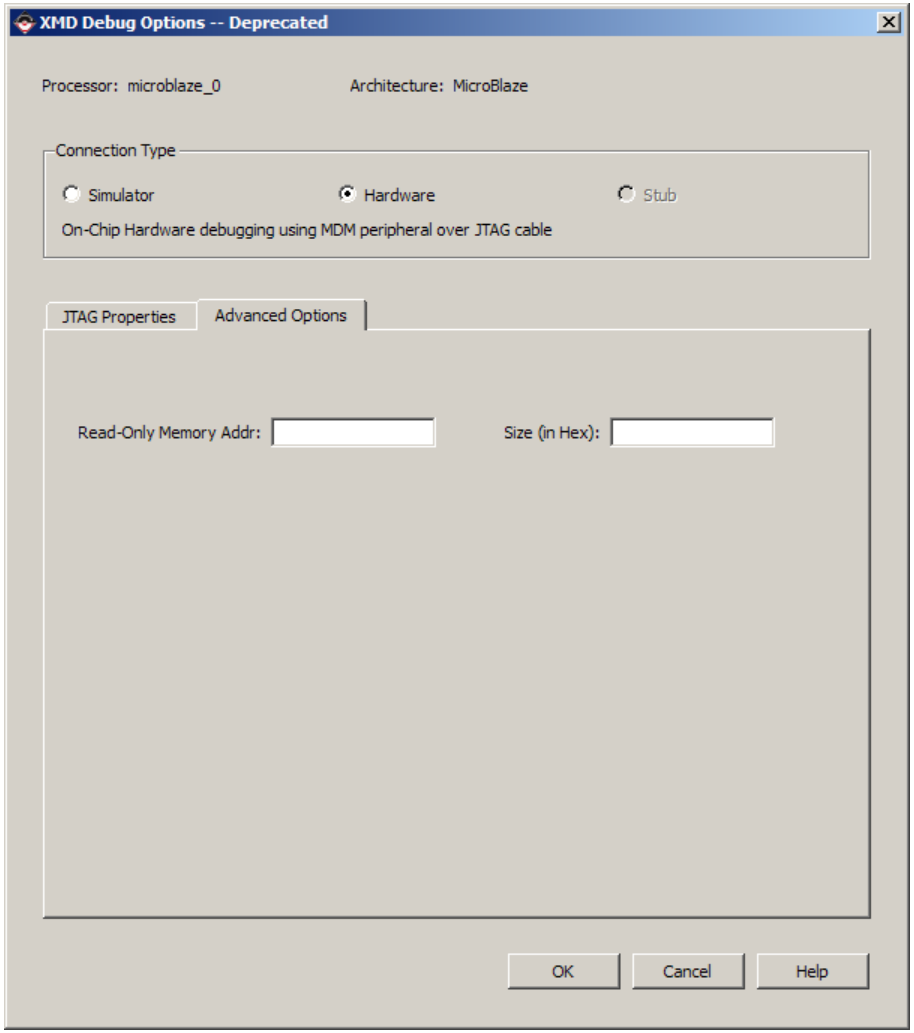


Note: Presentation applies to the ML505, ML506, and ML507

Loading a Bootloop ELF into the Block RAM

- The first time XMD runs on a project, the XMD Debug options must be set

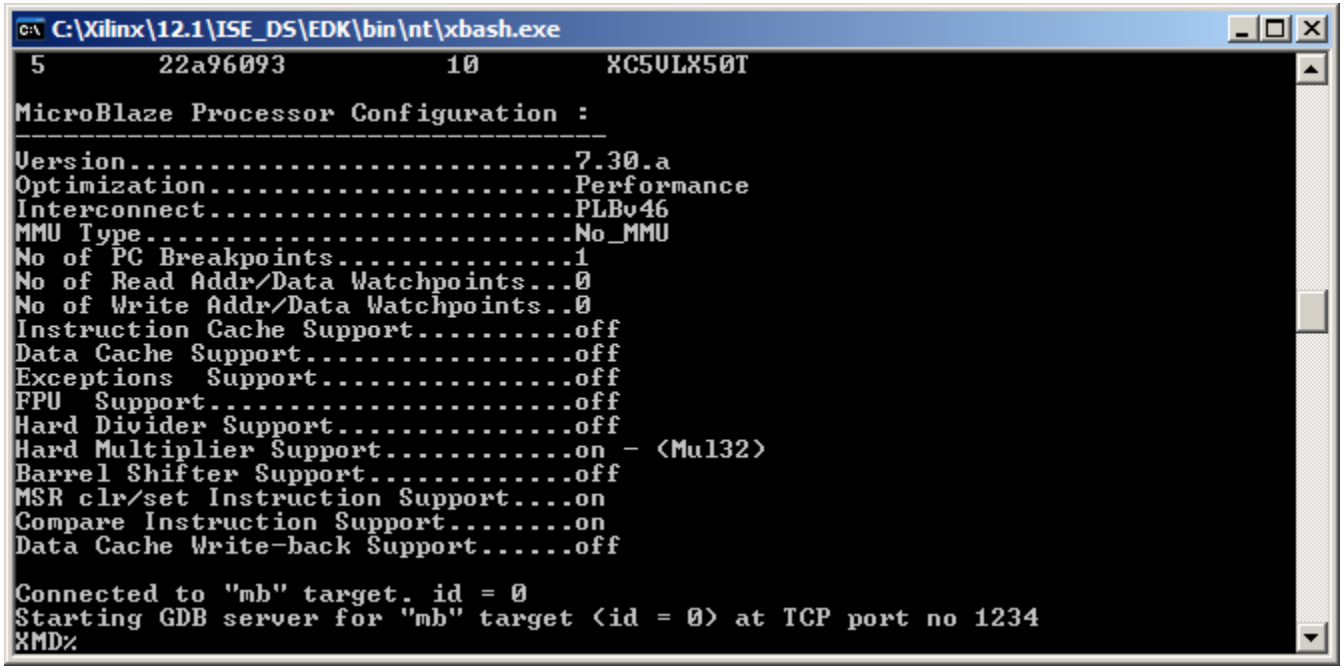




Note: Presentation applies to the ML505, ML506, and ML507

Loading a Bootloop ELF into the Block RAM

- XMD opens and connects to the processor, using the default options



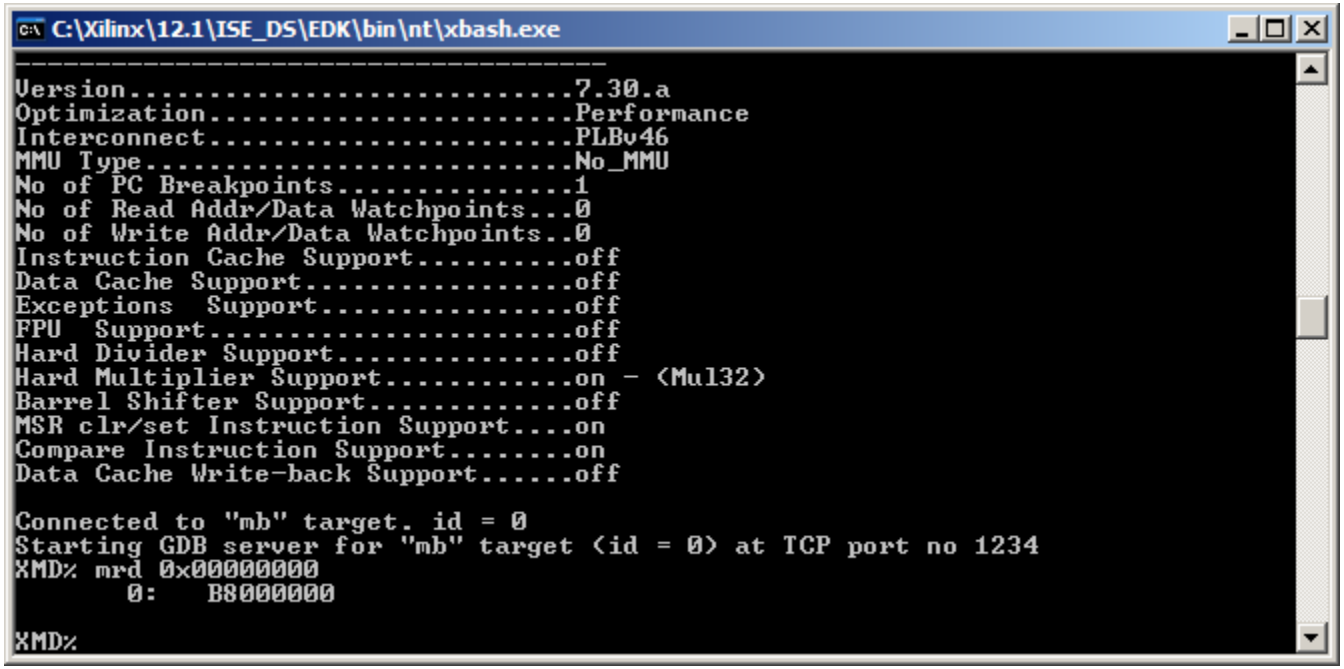
Note: Presentation applies to the ML505, ML506, and ML507

Loading a Bootloop ELF into the Block RAM

- To execute a memory read, type

  mrd 0x00000000

- This will read the memory address at the reset vector; the value should be 0xB8000000 as shown below



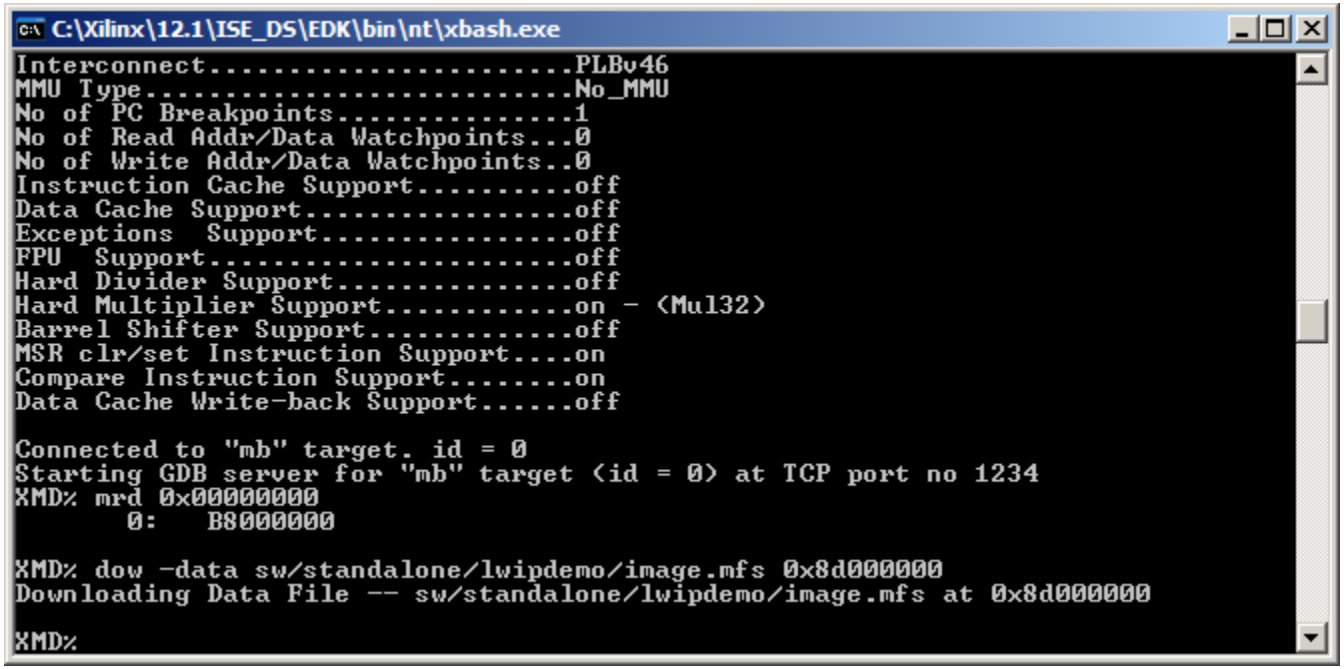
Note: Presentation applies to the ML505, ML506, and ML507

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Running the Lwipdemo Application

- **Download the MFS image:**

  dow -data sw/standalone/lwipdemo/image.mfs 0x8d000000



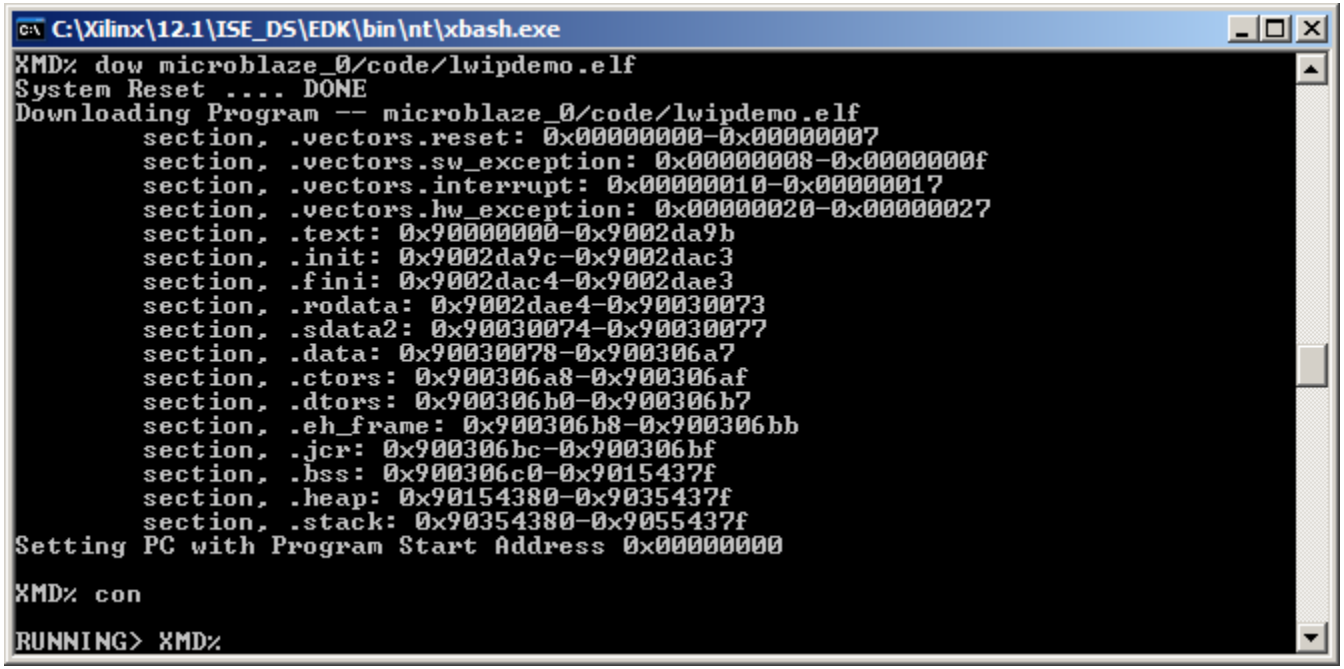
Note: Presentation applies to the ML505, ML506, and ML507

Running the Lwipdemo Application

- **Download and run the Lwipdemo Application:**

  dow microblaze_0/code/lwipdemo.elf

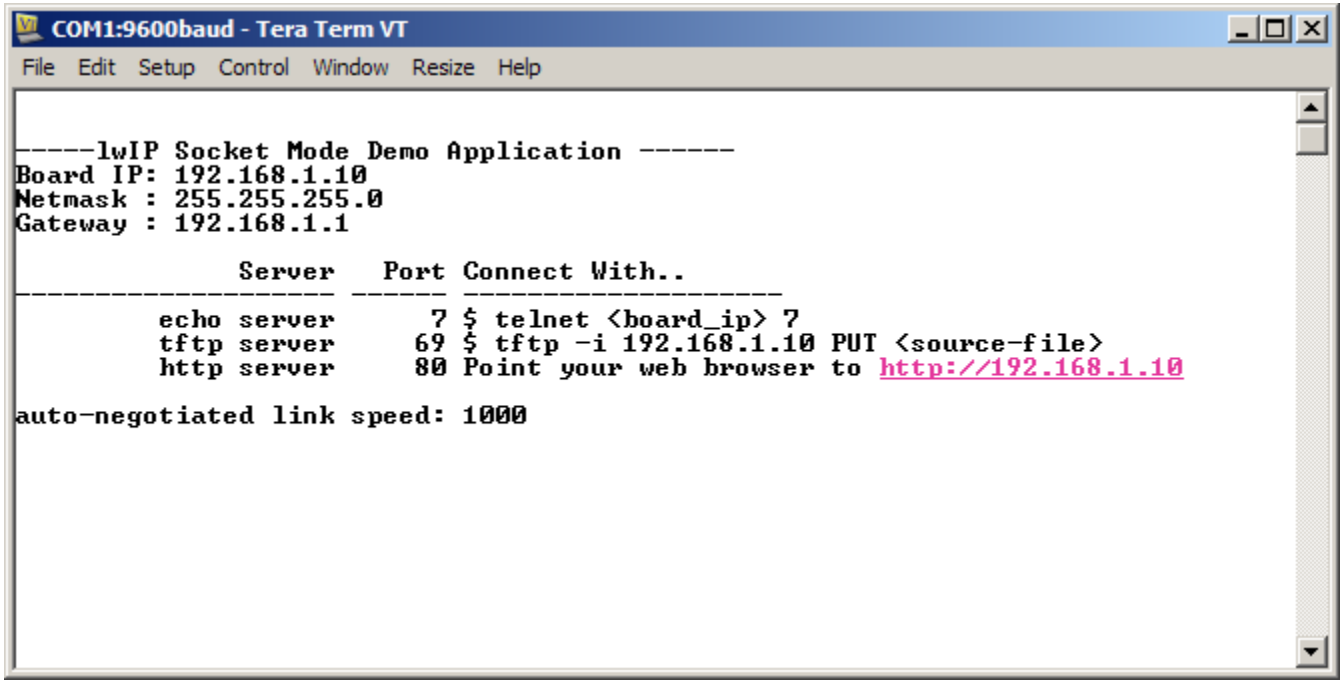
  con



Note: Presentation applies to the ML505, ML506, and ML507

Running the Lwipdemo Application

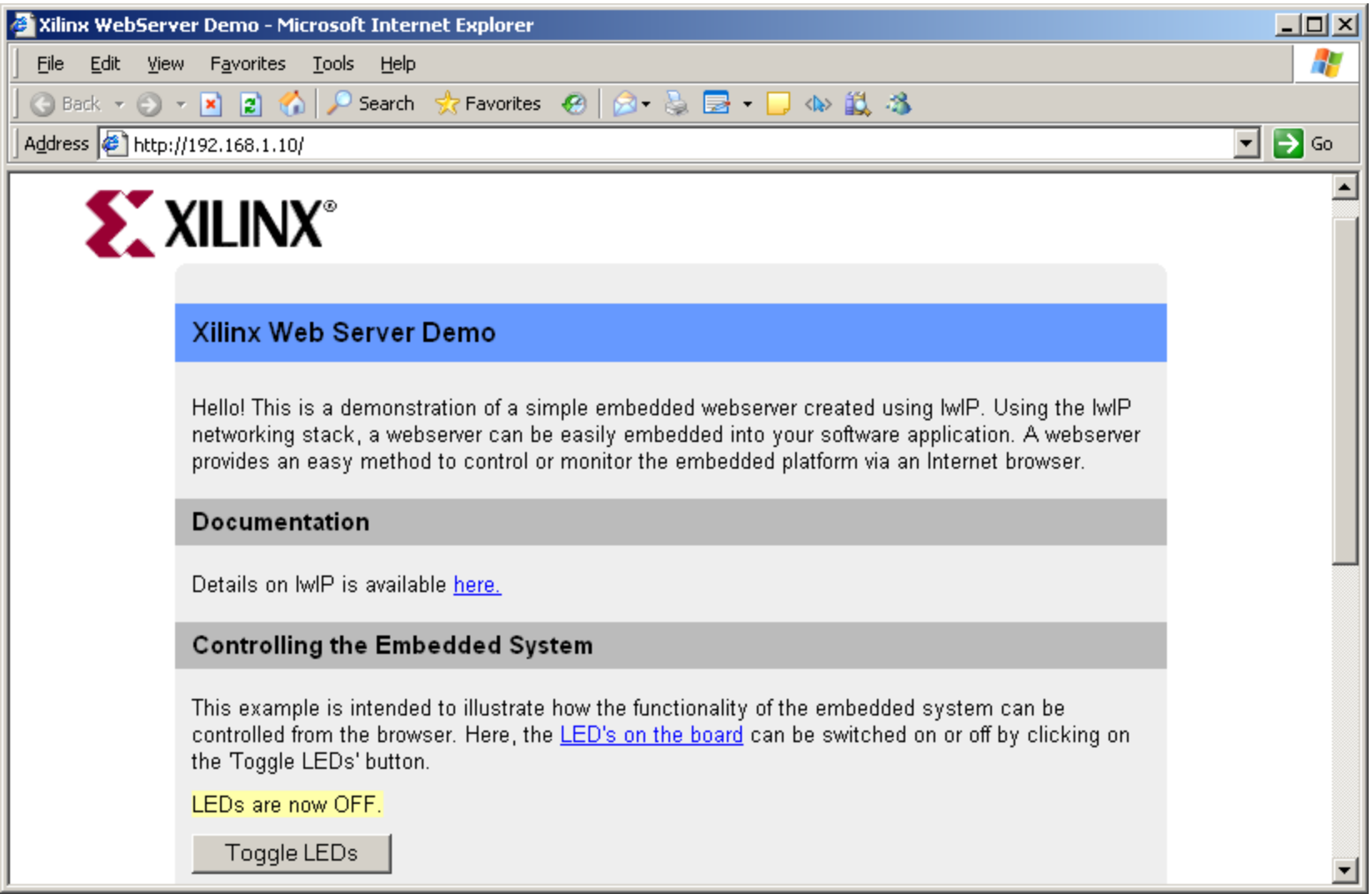
- View the output in the terminal window



Note: Presentation applies to the ML505, ML506, and ML507

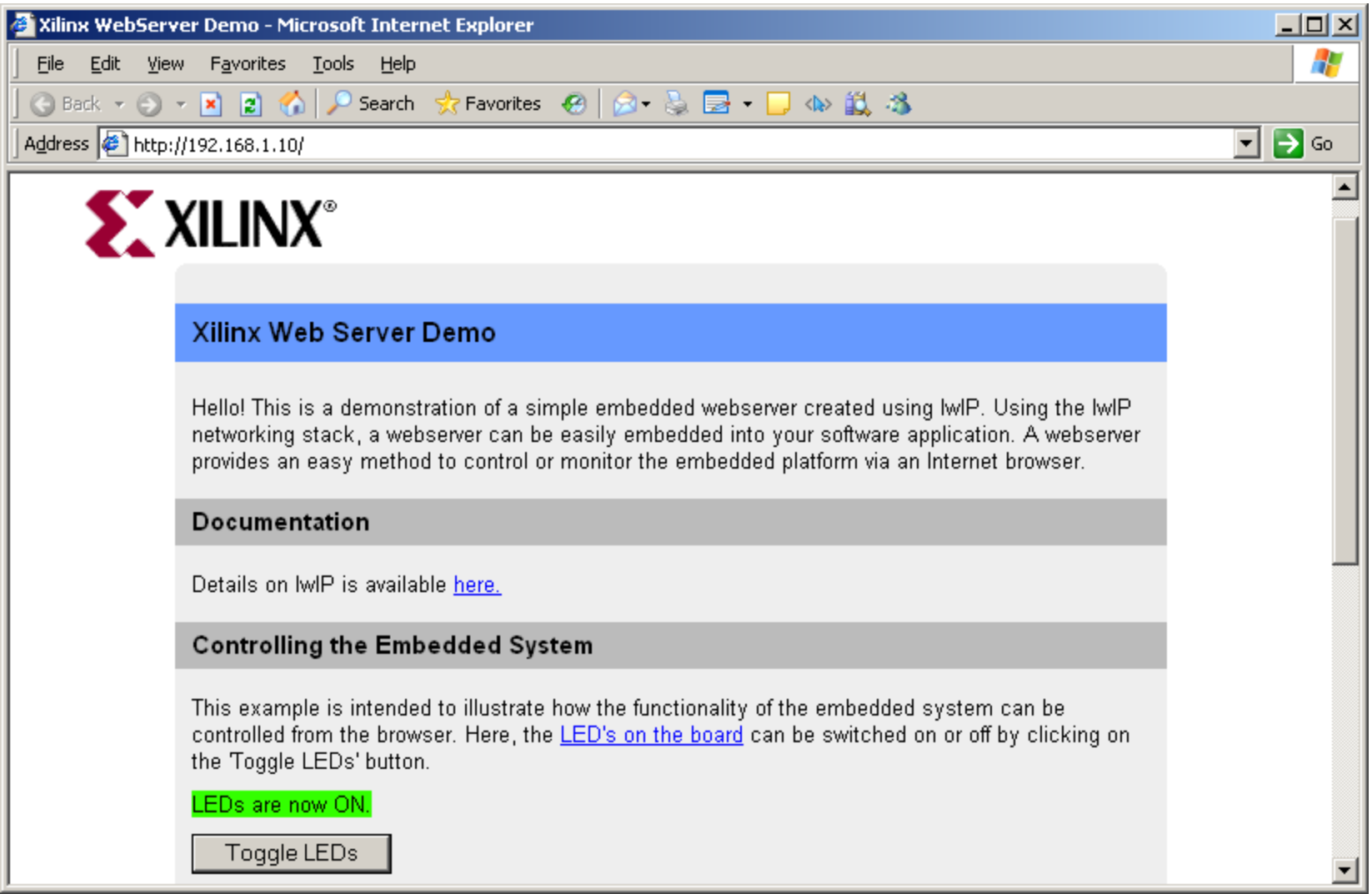
Running the Lwipdemo Application

- Open a web browser to address 192.168.1.10



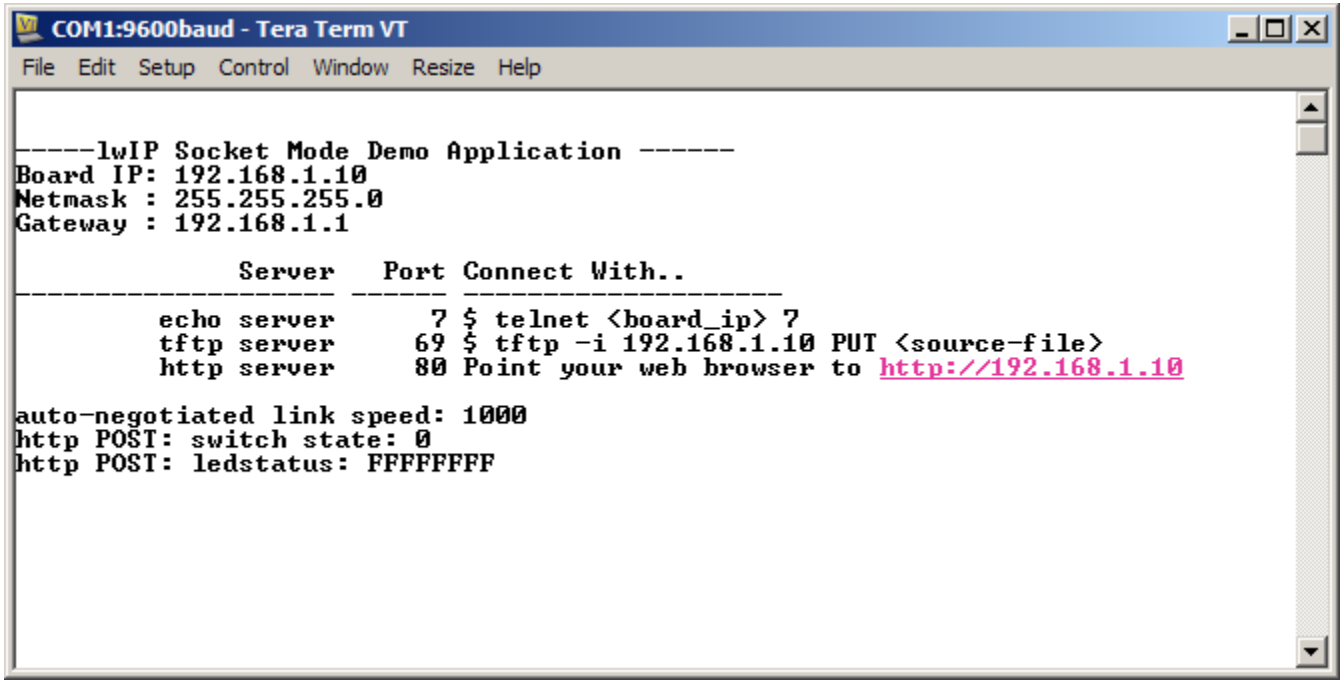
Running the Lwipdemo Application

- Click the Toggle LEDs button; view change on ML505



Running the Lwipdemo Application

- The Lwipdemo application shows the web transaction for the button push

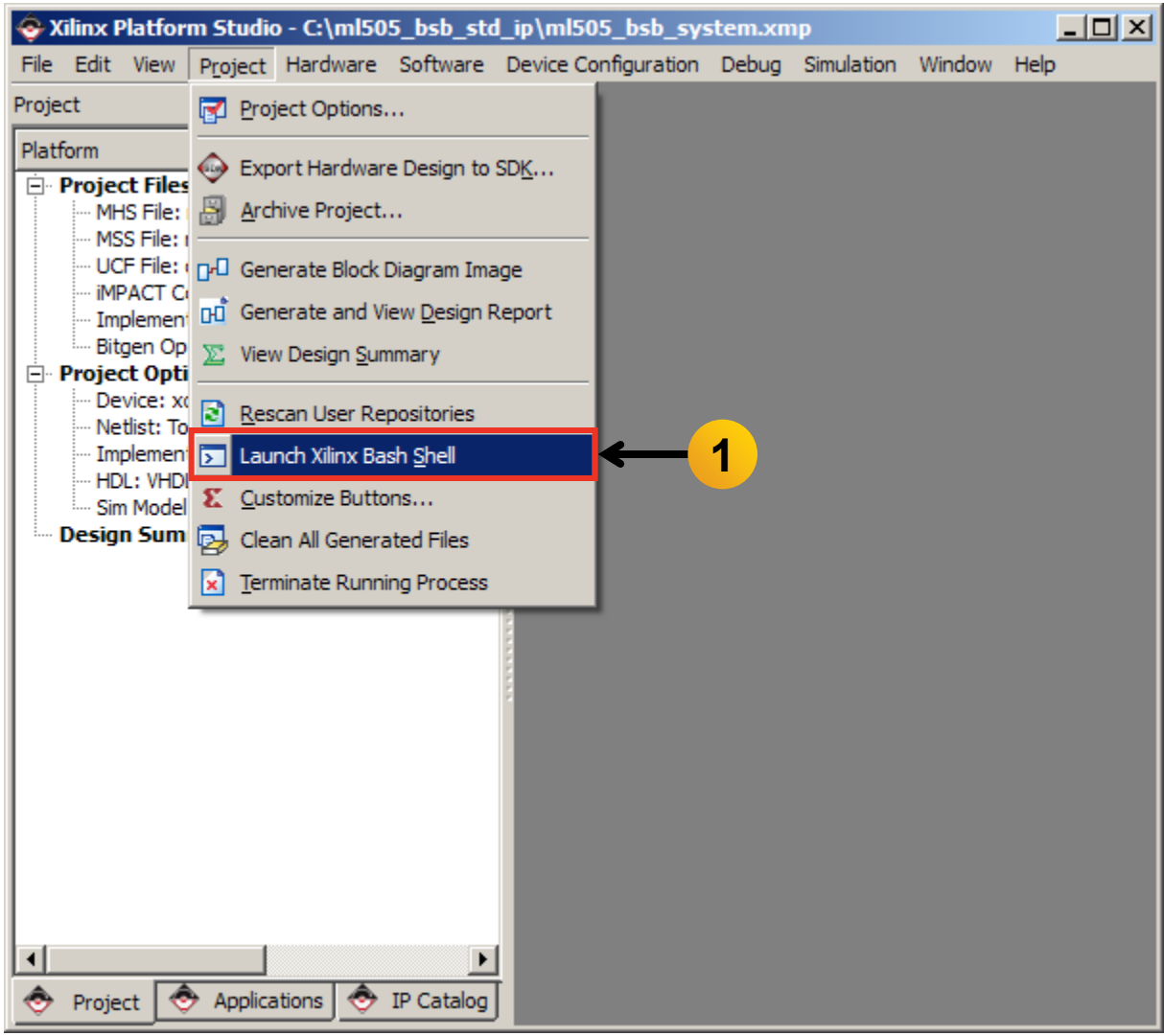


Note: Presentation applies to the ML505, ML506, and ML507

Create an ACE File

Create an ACE File

- **Open an EDK shell**
  - Select **Project → Launch Xilinx BASH Shell** (1)



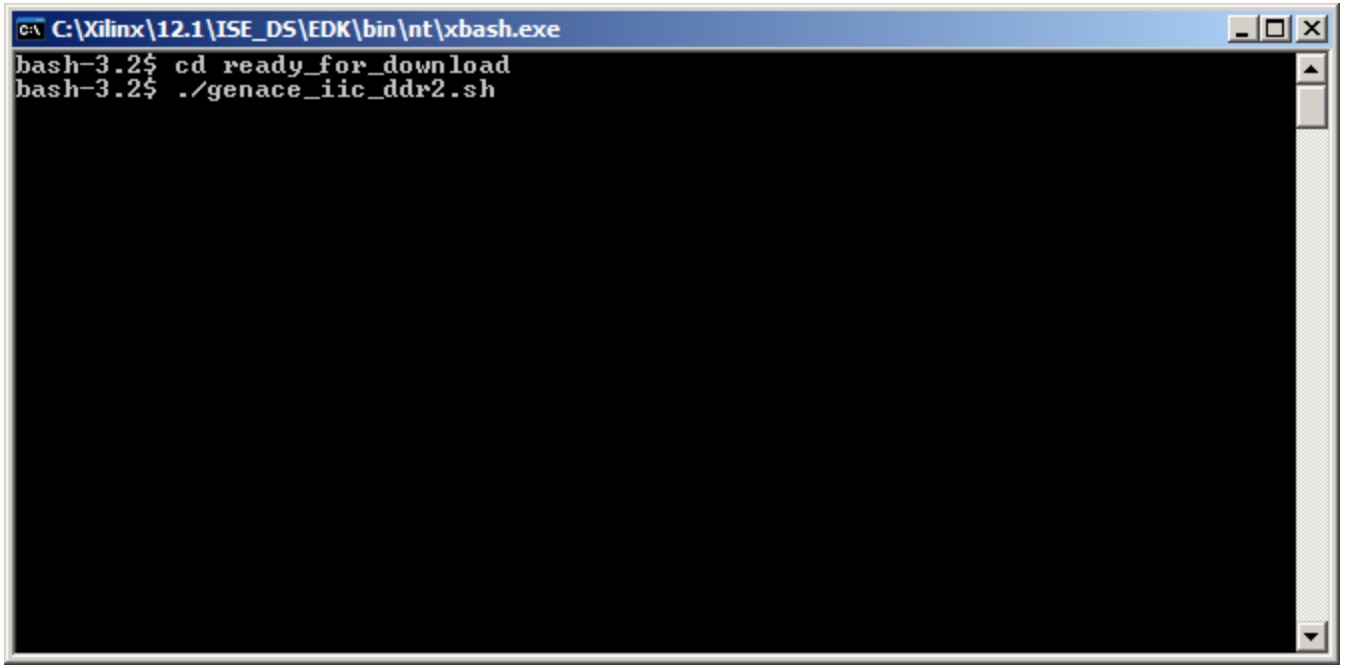
Note: Presentation applies to the ML505, ML506, and ML507

Create an ACE File

- At the bash prompt, type (1):

  cd ready_for_download

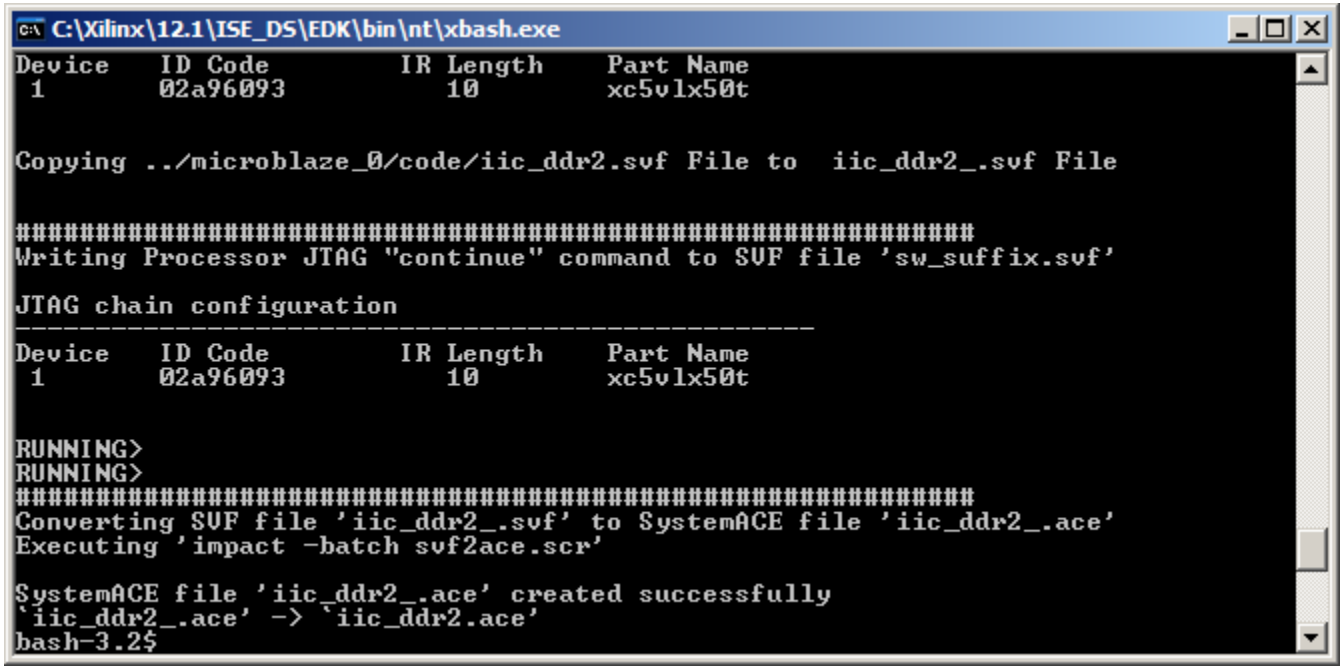
  ./genace_iic_ddr2.sh



Note: Presentation applies to the ML505, ML506, and ML507

Create an ACE File

- **This creates a concatenated (HW+SW) ACE file**
  - Input: iic_ddr2.elf, download.bit
- **genace_iic_ddr2.sh uses XMD and a genace.tcl script with ML505 appropriate options to generate an ACE file**



Note: Presentation applies to the ML505, ML506, and ML507

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Run ACE File

- **Copy iic_ddr2.ace to the ML50X\cfg6 directory on your CompactFlash card**
  - Important: Delete any existing ace files in this cfg6 directory
  - Note: Use a CompactFlash reader to mount the CompactFlash as a disk drive

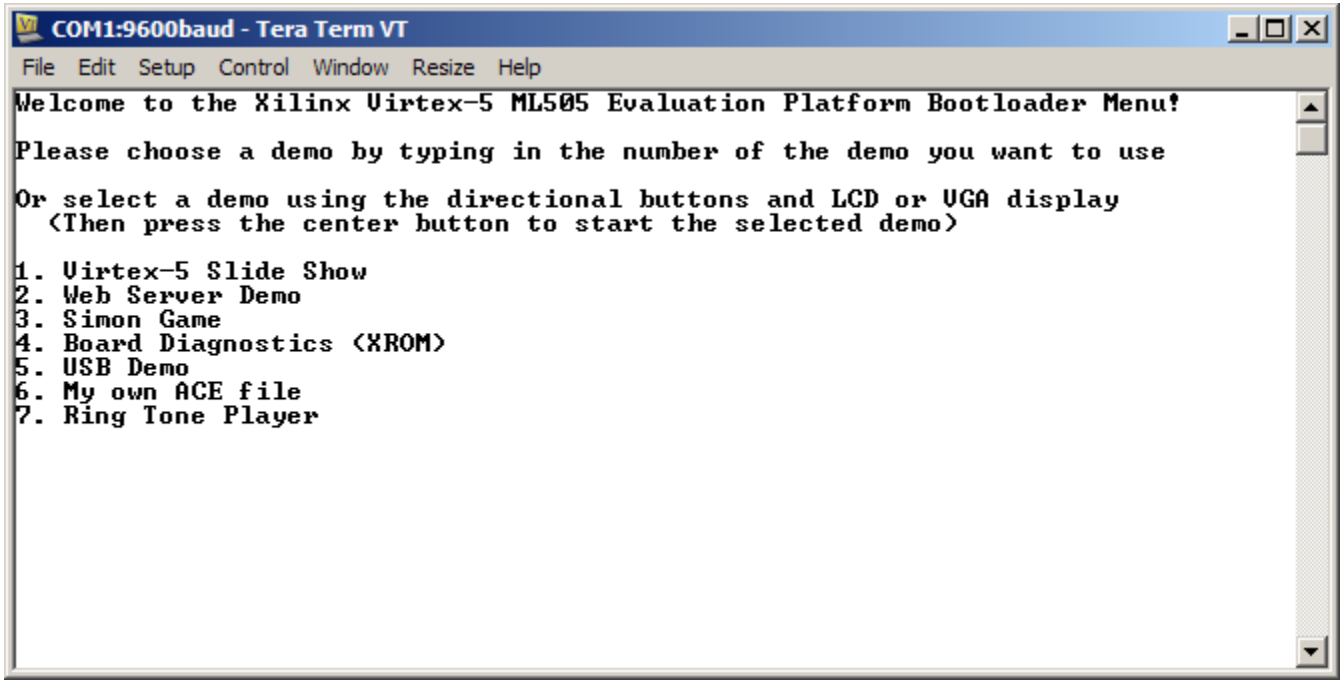




Note: Presentation applies to the ML505, ML506, and ML507

Run ACE File

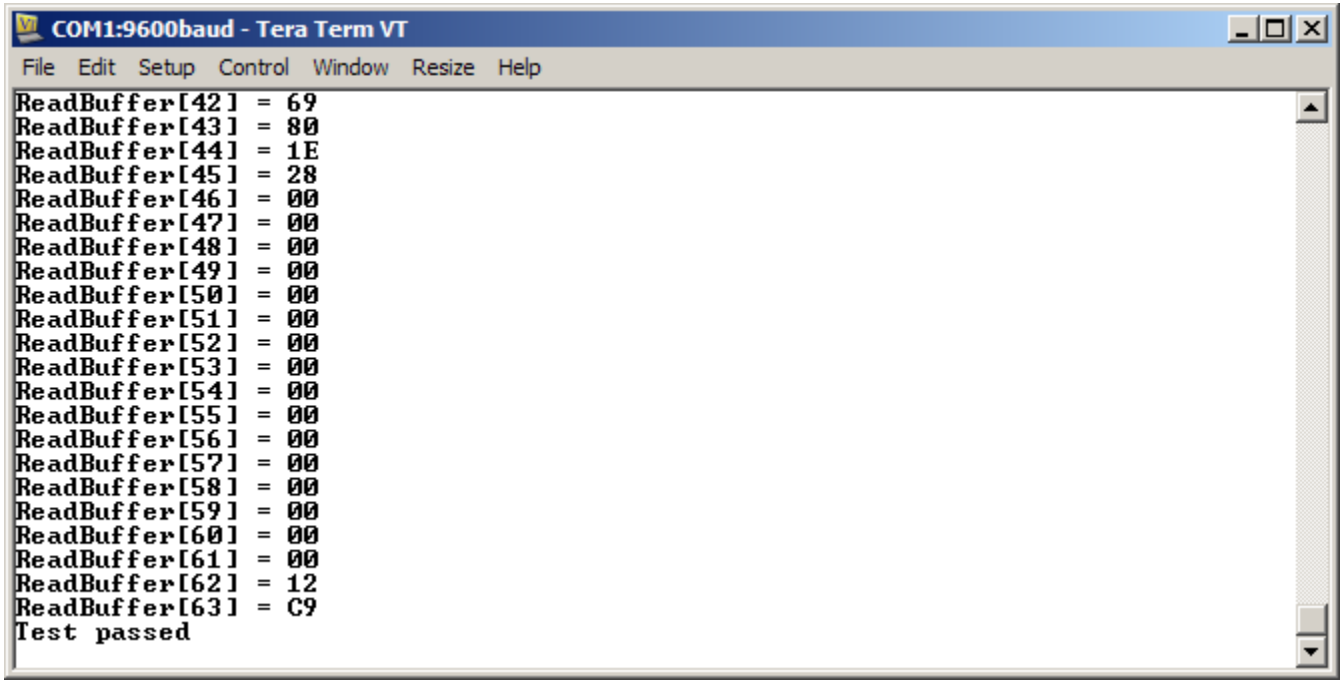
- **Use the new ACE file**
  - Eject the CompactFlash from your PC and insert it back into the ML505
  - Type **6** to run the newly created ACE file



Note: Presentation applies to the ML505, ML506, and ML507

Run ACE File

- iic_ddr2 output after booting ACE file



Note: Presentation applies to the ML505, ML506, and ML507

References

References

- **Virtex-5**
  - Virtex-5 FPGA Family
    http://www.xilinx.com/products/virtex5/index.htm
- **Platform Studio**
  - Embedded Development Kit (EDK) Resources
    http://www.xilinx.com/tools/platform.htm
  - Embedded System Tools Reference Manual
    http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/est_rm.pdf
  - EDK Concepts, Tools, and Techniques
    http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/edk_ctt.pdf

Documentation

Documentation

- **ML505/506/507 Documentation**
  - ML505 Overview
    http://www.xilinx.com/ml505
  - ML506 Overview
    http://www.xilinx.com/ml506
  - ML507 Overview
    http://www.xilinx.com/ml507
  - ML505/506/507 Evaluation Platform User Guide – UG347
    http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf
  - ML505/506/507 Getting Started Tutorial – UG348
    http://www.xilinx.com/support/documentation/boards_and_kits/ug348.pdf
  - ML505/506/507 Reference Design User Guide – UG349
    http://www.xilinx.com/support/documentation/boards_and_kits/ug349.pdf