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ALL PROGRAMMABLE™

System Design on Zynq using SDSoC

SDx 2018.1

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Objectives

- After this hour, you will be able to:
  - Identify the basic building blocks of the Zynq architecture processing system (PS)
  - Describe the SDSoC development environment
  - List some examples of SDSoC use cases
  - List some of the benefits of using SDSoC
  - Identify some of the underlying tools the SDSoC development environment uses
  - Describe the SDSoC tool development flow
  - List steps involved in creating an SDSoC project

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Outline

- *Zynq All Programmable SoC (AP SoC)*
- Processor Peripherals and Interfaces
- *SDSoC Development Environment*
- SDSoC Development Flow
- SDSoC Project Creation
- Summary

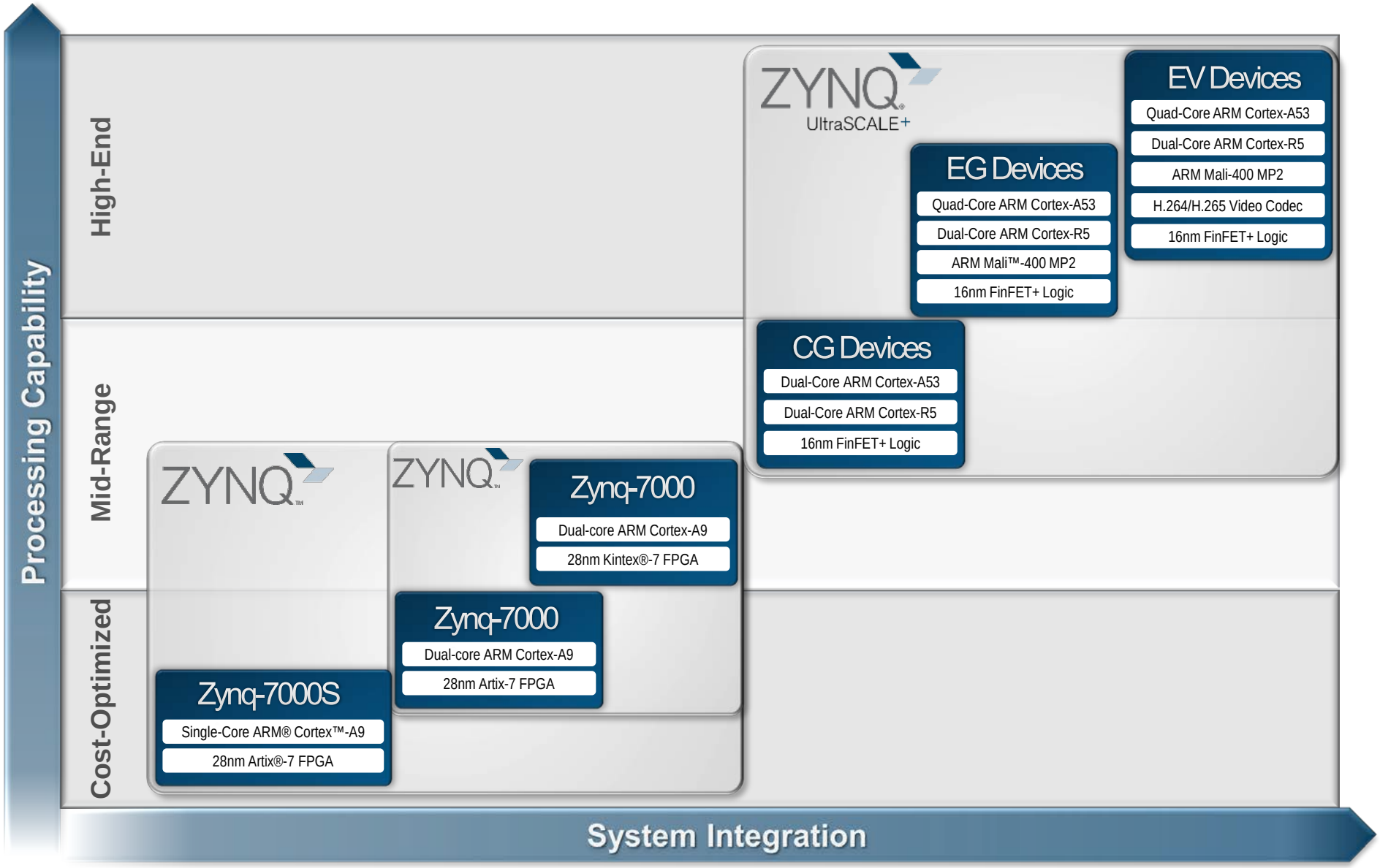
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The PS and the PL

- The Zynq-7000 AP SoC architecture consists of two major sections
  - PS: Processing System
    - Dual ARM Cortex-A9 processor based (Single core versions available)
    - Multiple peripherals
    - Hard silicon core
  - PL: Programmable Logic
    - Shares the same 7 series programmable logic as
      - Artix™-based devices: Z-7010, Z-7015, and Z-7020 (high-range I/O banks only)
      - Single core versions: Z-7007S, Z-7012S, and Z-7014S
      - Kintex™-based devices: **Z-7030**, Z-7035, Z-7045, and Z-7100 (mix of high-range and high-performance I/O banks)

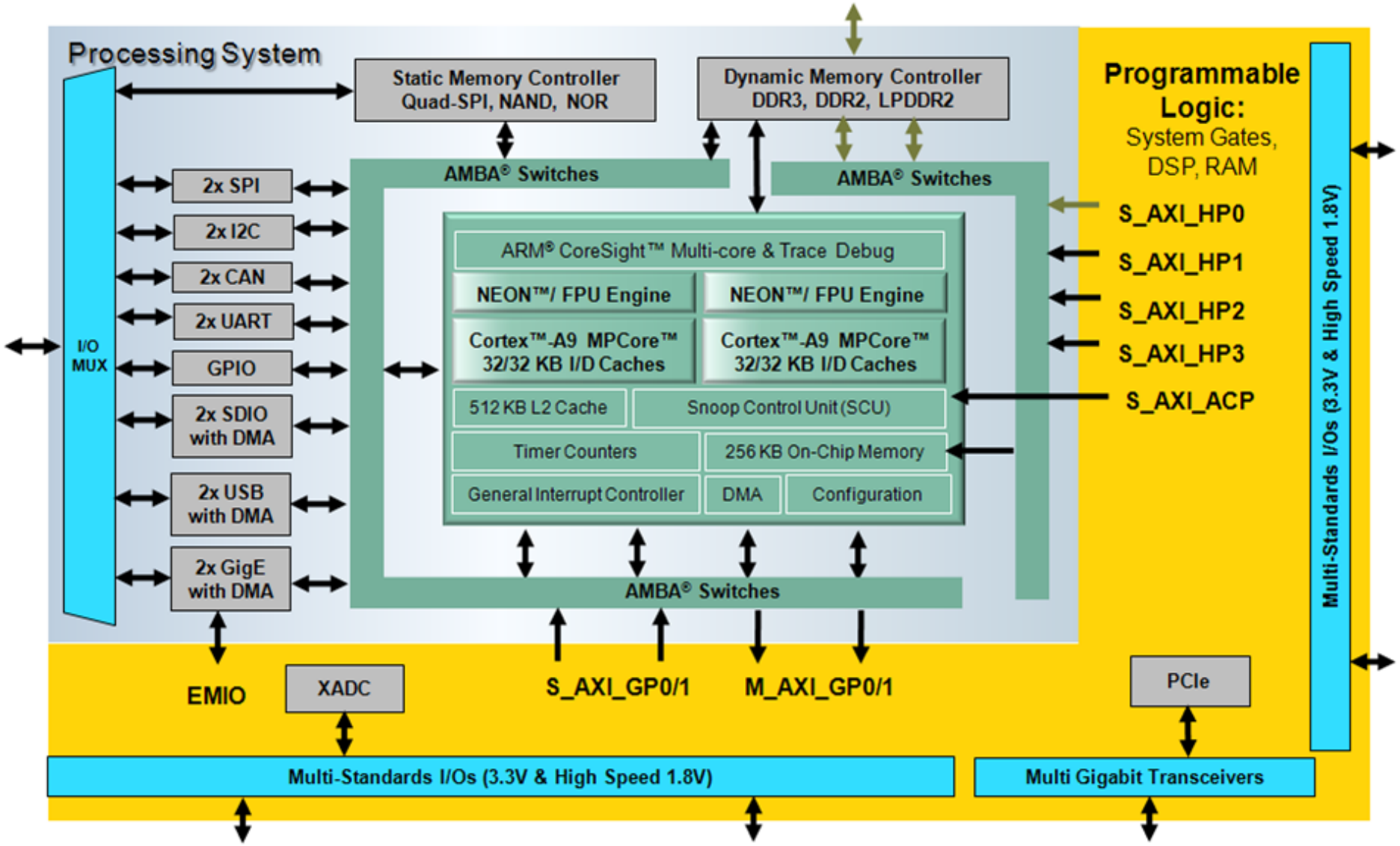
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Extending Scalability Across the Zynq Portfolio



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Zynq-7000 AP SoC Block Diagram



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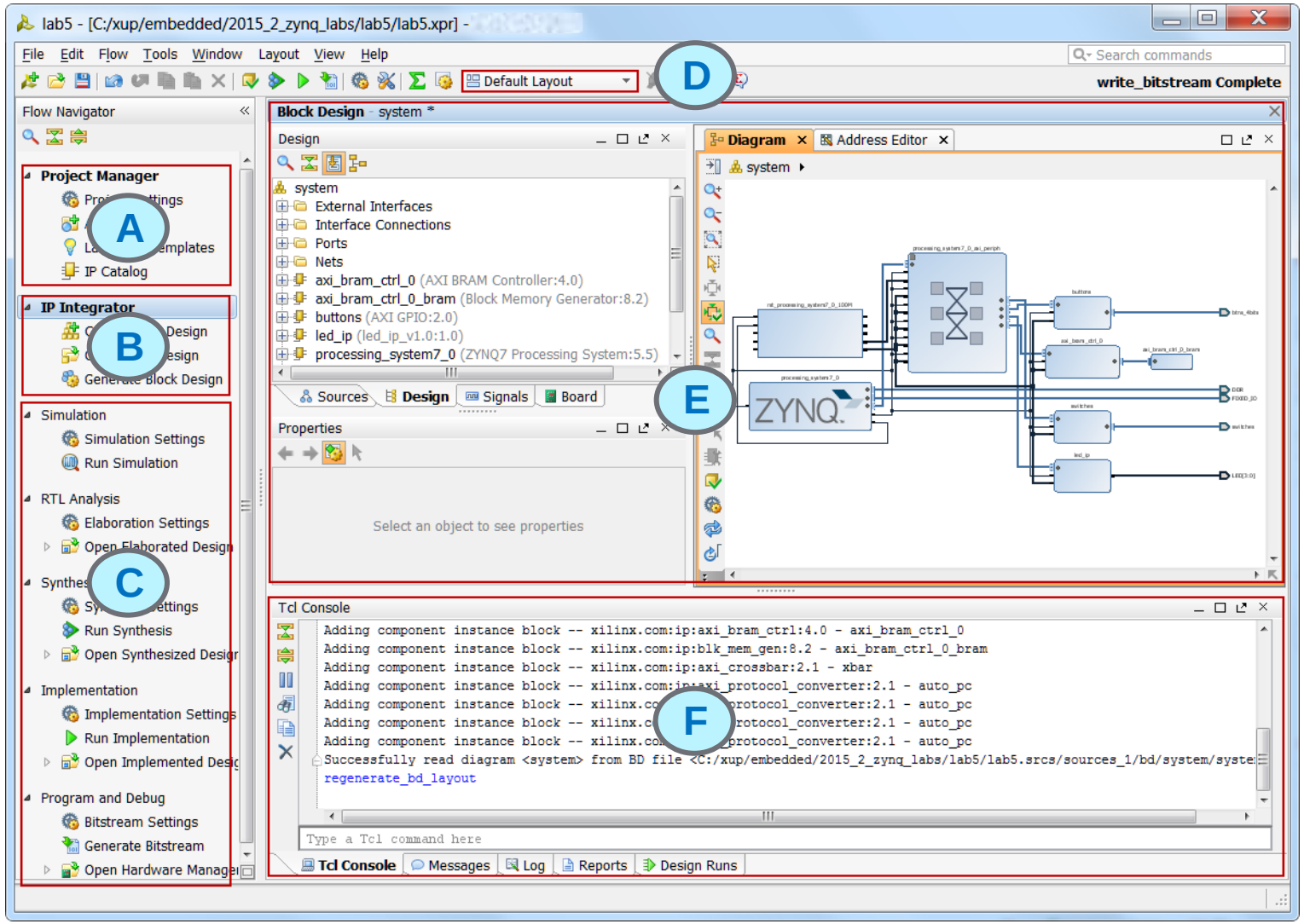
PS Components

- Application processing unit (APU)
- I/O peripherals (IOP)
  - Multiplexed I/O (MIO), extended multiplexed I/O (EMIO)
- Memory interfaces
- PS interconnect
- DMA
- Timers
  - Public and private
- General interrupt controller (GIC)
- On-chip memory (OCM): RAM
- Debug controller: CoreSight

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Vivado View

- Customizable panels
  - A: Project Management
  - B: IP Integrator
  - C: FPGA Flow
  - D: Layout Selection
  - E: Project view/Preview Panel
  - F: Console, Messages, Logs



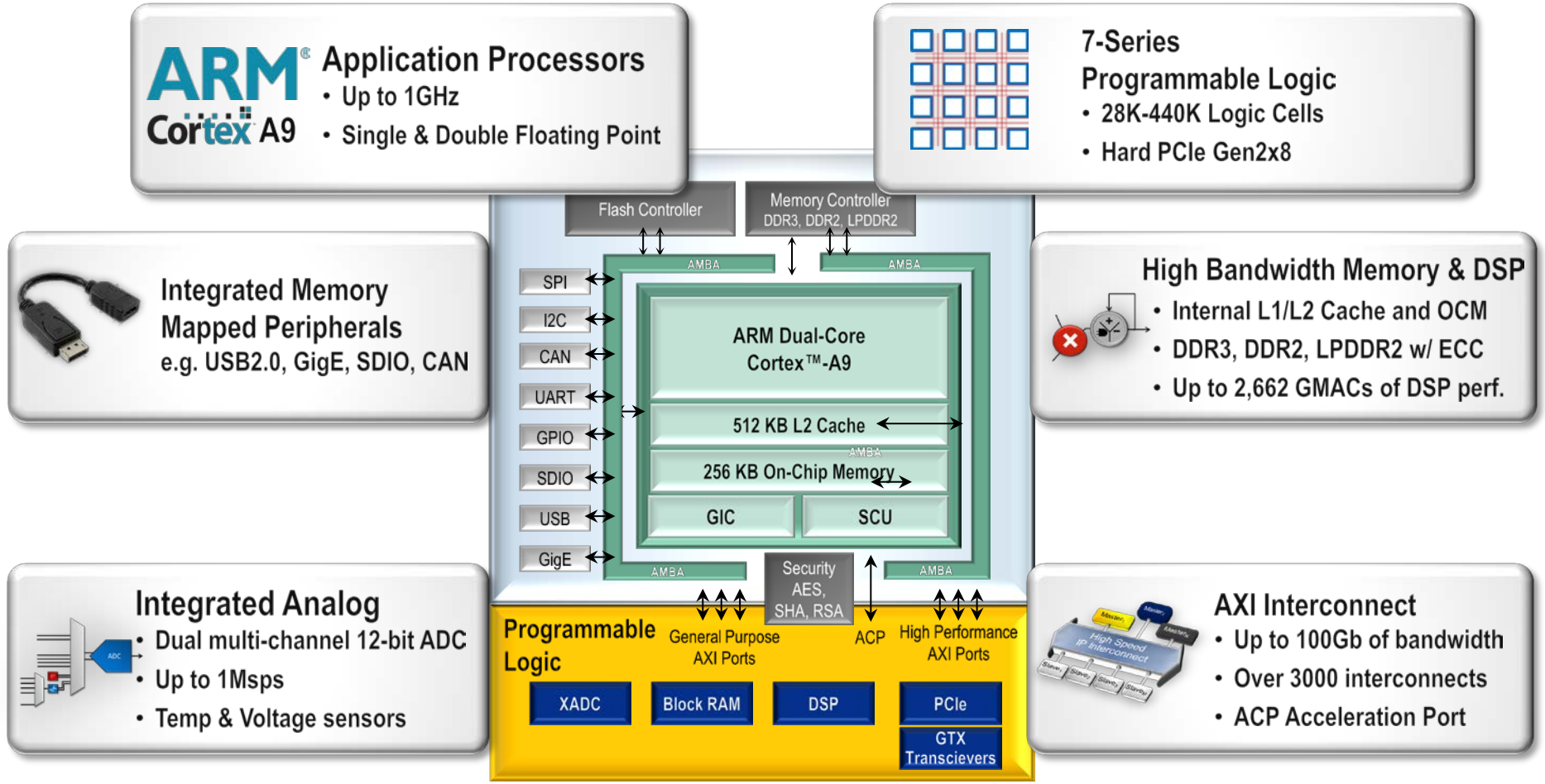
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Zynq-7000 All Programmable SoC Highlights



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SDSoC- Part of SDx

- Starting with 2016.3, SDx provides SDSoC - SDAccel Development Environment Common Infrastructure
  - Eclipse based IDE with support for project creation, emulation, performance estimation, implementation and debug
  - One-stop Reports View to access all reports
- SDSoC supports
  - Devices support
    - Zynq-7000 and Zynq UltraScale+ MPSoC support
  - ARM compiler tool chain support
    - Linaro-based gcc 6.2-2016.11 32-bit and 64-bit tool chains
  - Target OS support
    - Linux (kernel 4.9, Xilinx branch xilinx-v2017.2_sdsoc), bare-metal and FreeRTOS 8.2.3
  - QEMU and RTL co-simulation (Zynq target, Linux Host OS only, beta for Windows)
  - OpenCL compilation flows are now supported for Zynq and Zynq UltraScale+ MPSoC devices

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SDSoC Development Environment

- What is it?
  - SDSoC provides a familiar embedded C/C++ application development experience including
    - An easy to use Eclipse IDE
    - A comprehensive design environment for heterogeneous Zynq SoC and MPSoC
    - C/C++ full-system optimizing compiler
  - SDSoC enables function acceleration in PL with a click of button using various technologies
    - Vivado IPI
    - Vivado HLS
    - SDK
    - Profiler
  - SDSoC provides infrastructure to combine processing system, accelerators, data movers, signaling, and drivers
    - Whereas the Vivado HLS tool only build the RTL; connectivity, supporting IP drivers etc. must be supplied by the designer

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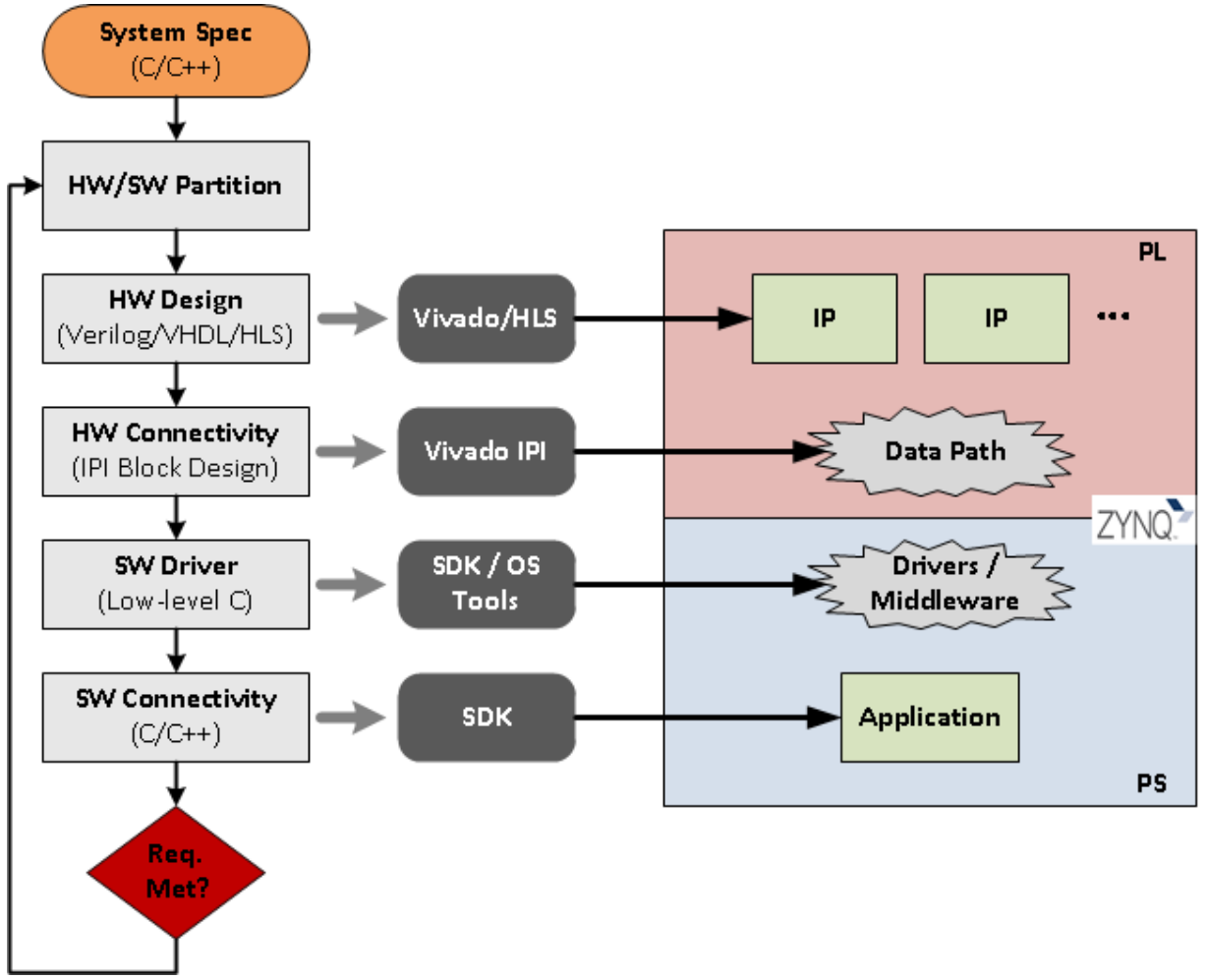
Benefits of SDSoC Development Environment

- Shorter development cycles
  - Estimation shows improvement over software-only solution for system and accelerators
  - Iterative improvement can be made at early stages of development without the need to build hardware
- Simplified interface and partitioning between hardware and software
  - Software-based flow vs RTL
    - User interfaces with software-only tools; hardware management is abstracted
    - Removes much of the hardware/software distinction and throw-over-the-wall effect
- Automated initial design
  - Users can tweak code at macro- and micro-architectural levels
  - Designers still have manual control over the constructed Vivado HLS tool and Vivado Design Suite projects

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Development Flow Without SDSoC

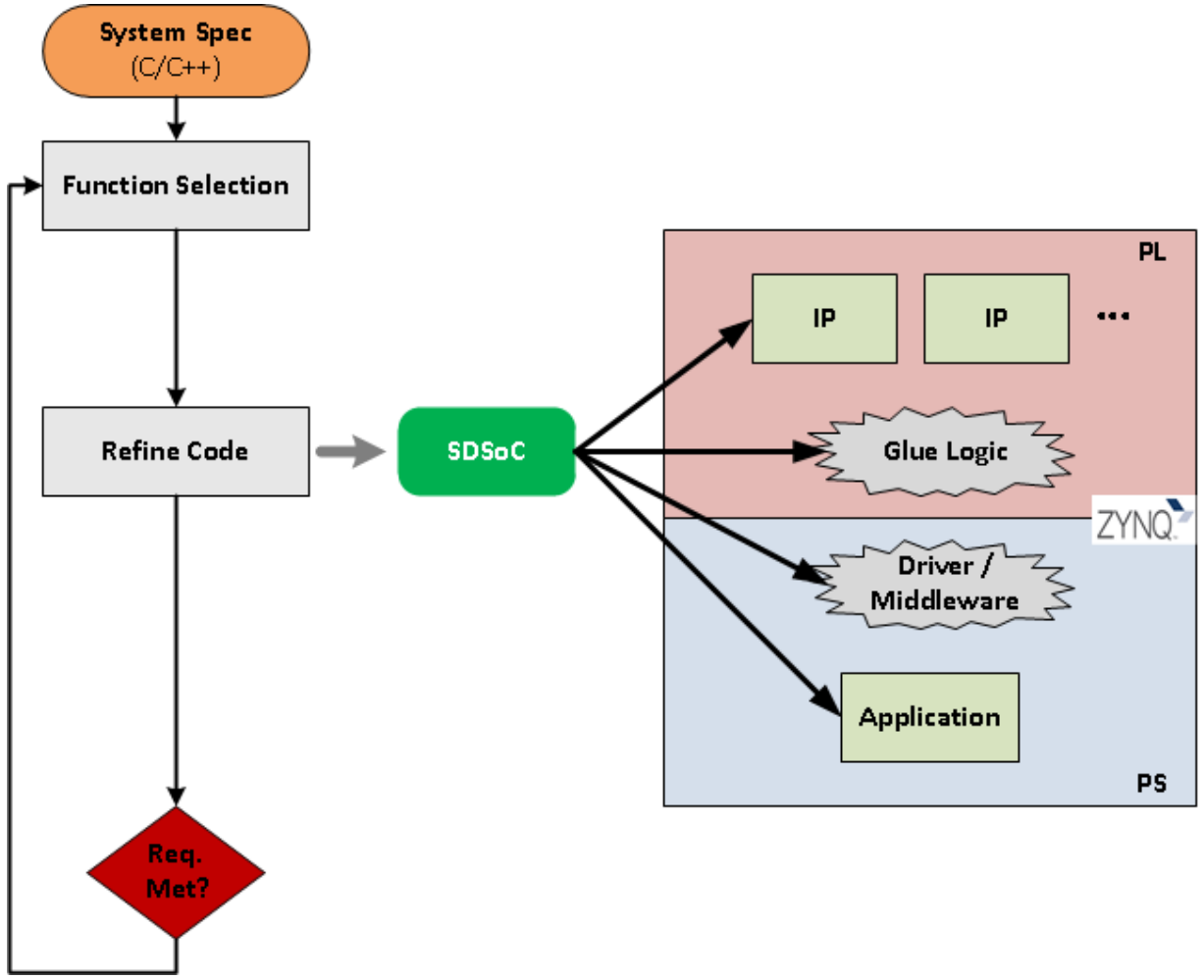
- **Overall process requires expertise at all steps in the development process**
  - Various hardware design entries
  - Hardware connectivity at system level
  - Driver development to drive custom hardware
  - Integrating with application and target OS



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Development Flow with SDSoC

- **SDSoC development environment consolidates a multi-step/multi-tool process into a single tool and reduces hardware/software partitioning to simple function selection**
  - Code typically needs to be refined to achieve optimal results



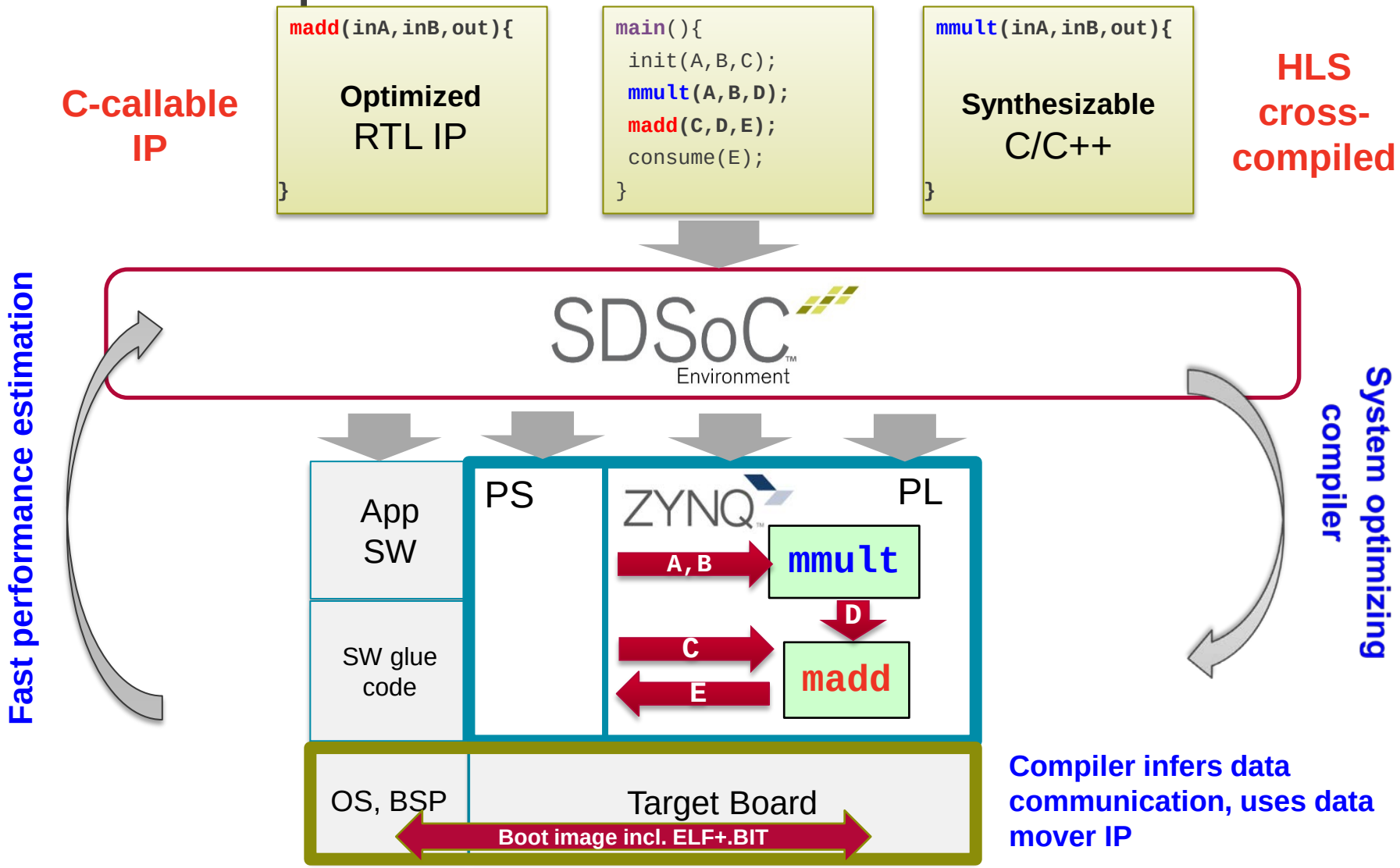
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SDSoC Development Flow



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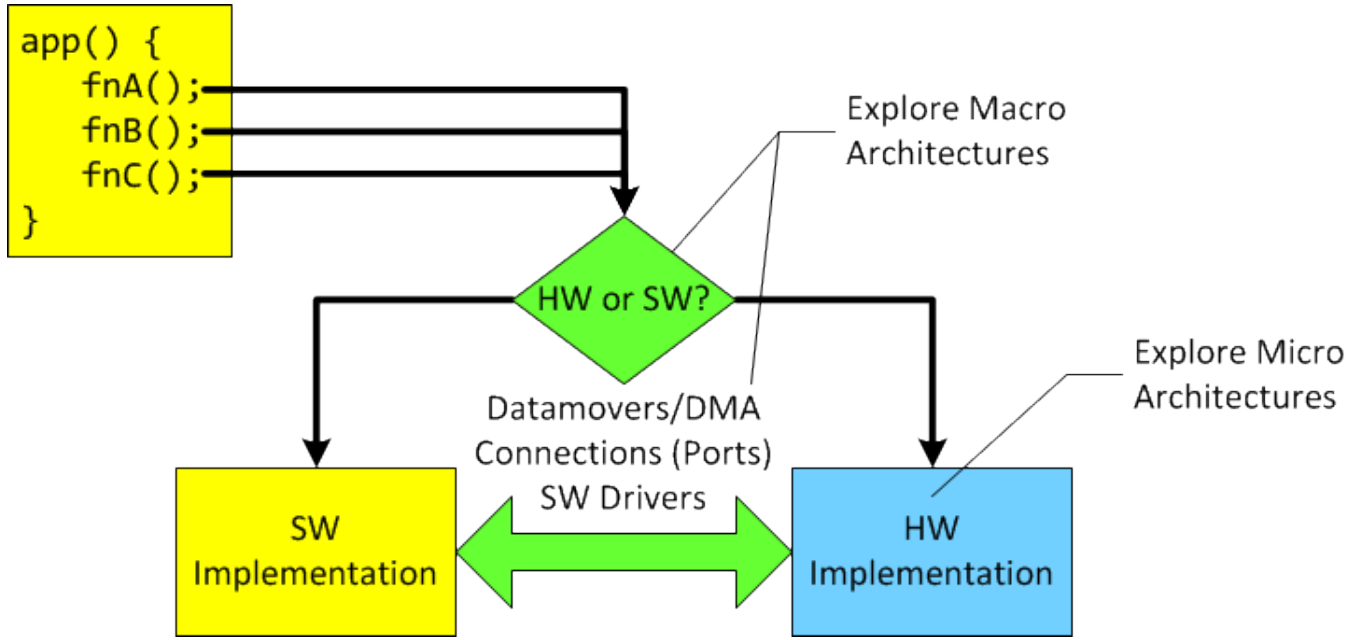
Users must keep in mind

- Tools abstract away many of the challenges
  - Novices can attain some basic level of results
  - Full performance only comes with understanding
- The Vivado HLS tool
  - The SDSoC development environment does not perform any code optimizations
  - The Vivado HLS tool skills are very important to achieve optimal performance
  - Understanding the Zynq AP SoC architecture is also beneficial
- C/C++
  - Tools are GNU based
  - New C learners should follow a non-SDSoC development environment flow
  - Familiarity with refactoring for the SDSoC development environment

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System-level Considerations

- What gets accelerated?
- How is software implemented in hardware?
  - Is hardware design expertise available?
- How will software and hardware talk to each other?
- Will it meet performance requirements the first try?
  - What changes are required at the macro/micro-architecture levels



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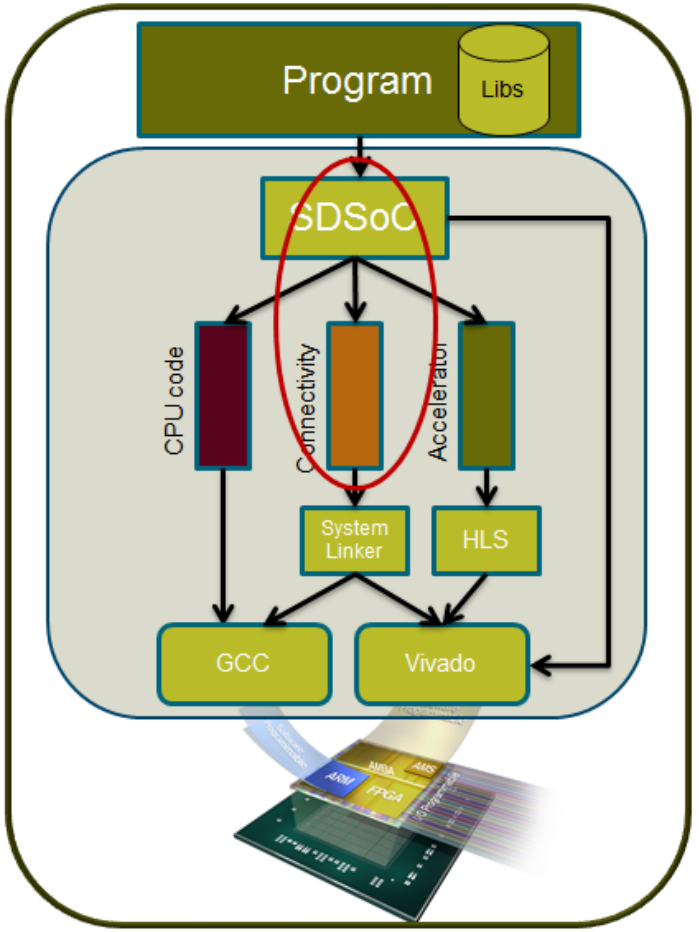
Candidate for an Accelerator

- Not every function can be a candidate for acceleration
  - For example, pre-compiled code, some user libraries, OS services, etc.
- Computationally intensive algorithms are ideal candidates
  - Profiling results help identify performance bottlenecks
    - Just because a function takes a long time, it is not automatically a candidate
  - Slight code modifications (or pragmas) effect the microarchitecture of the accelerator
- Trade-off between data movement costs and acceleration benefits should be considered

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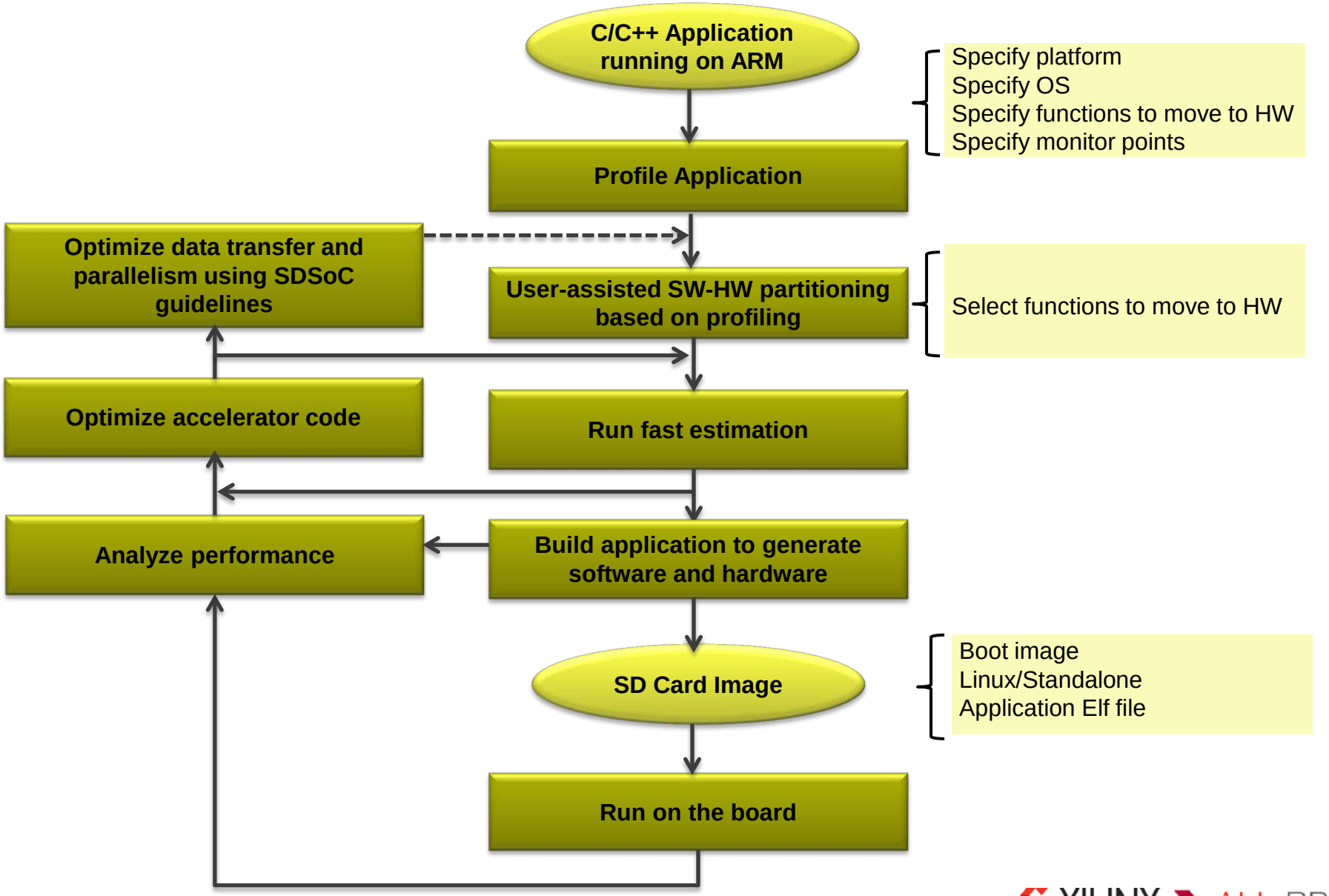
Simplifying Hardware/Software Partitioning

- SDSoC simplifies the process of identifying and accelerating functions
  - Integrates profiling tools
  - Provides libraries for accurate timing measurements
  - *User selects functions* to accelerate
  - Estimates hardware speed-up
- *Automated* acceleration is achieved through
  - Advanced analysis of code using specialized compilers
  - Assistance of user-specified pragmas
  - Extension of a predefined hardware platform
- Hardware platforms packaged with the environment and from third parties
  - Environment extends platform, providing additional capabilities



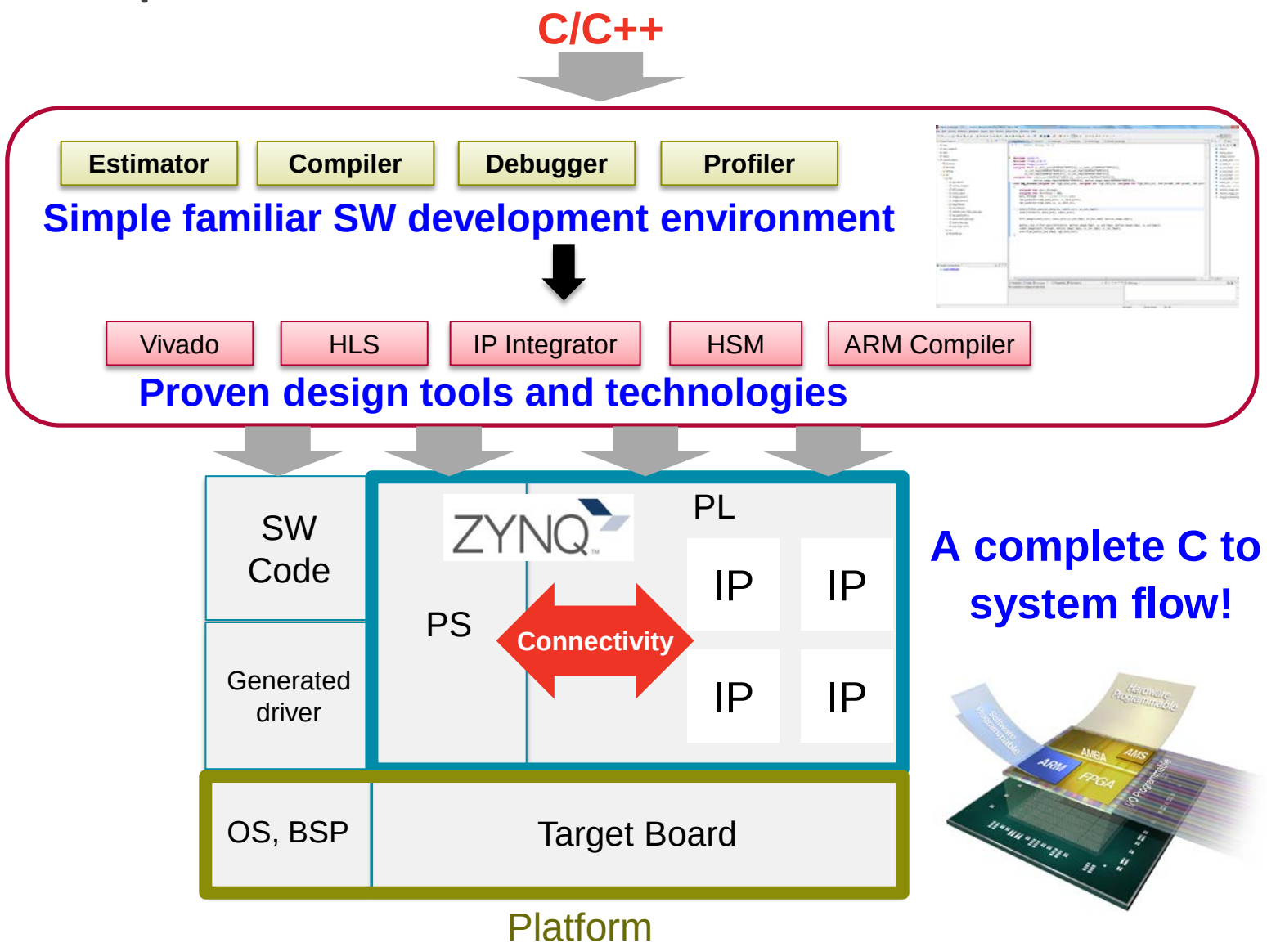
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Development Flow



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SDSoC: Complete End-to-End Flow

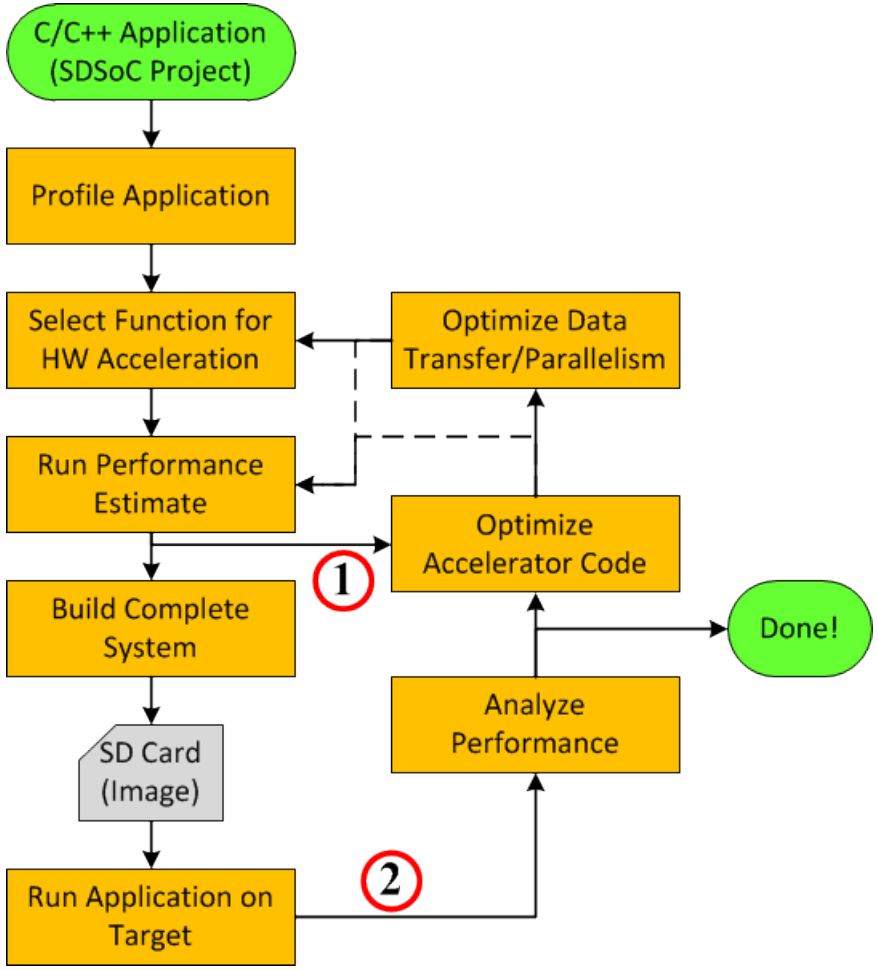


A complete C to system flow!

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Development Flow

- **Without hardware generation, the SDSoC development environment acts like a normal C/C++ IDE**
- **With SDSoC it starts with a pure software system and ends with an accelerated SW/HW system**
  - Developers select C functions for hardware acceleration
- **Estimate provides quick-turns to get architectures close**
  - Used in early development
- **Release generates full hardware/software products**
  - For later and final stages of development



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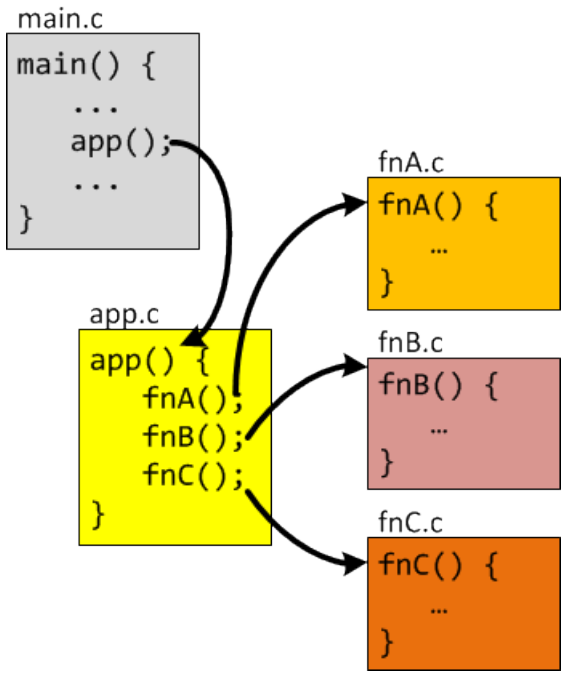
Profiling the Application

- The goal of offloading software to hardware is to improve overall system performance
- Finding software eligible for acceleration follows general software optimization practices
  - Profiling yields the necessary data by summarizing where execution time was spent
- The SDSoC development environment includes the TCF profiling tool
  - No code instrumentation or special recompiling required
  - Profiling results show percentage of time spent in functions relative to a total execution time
- For absolute timing measurements *sds_lib* offers some functions for collecting system timer values
  - Timer resource must be available and code must be changed to incorporate timer functions

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Accelerating Software Functions

- Individual functions must be marked for acceleration
  - Functions selected for acceleration are "hardware functions“
    - Hardware functions can contain sub-functions
  - Refactoring required if critical points are not isolated as functions
  - Each function becomes an individual piece of IP
- OS-based platforms have only one master thread communicates with all cores
- Restrictions
  - Only one function per file scope
    - Splitting of files may be required to accelerate multiple functions
  - Call to a hardware function must reside in a different file scope than the hardware function
  - Other tool limitations may apply
    - See Vivado HLS tool C/C++ guidelines



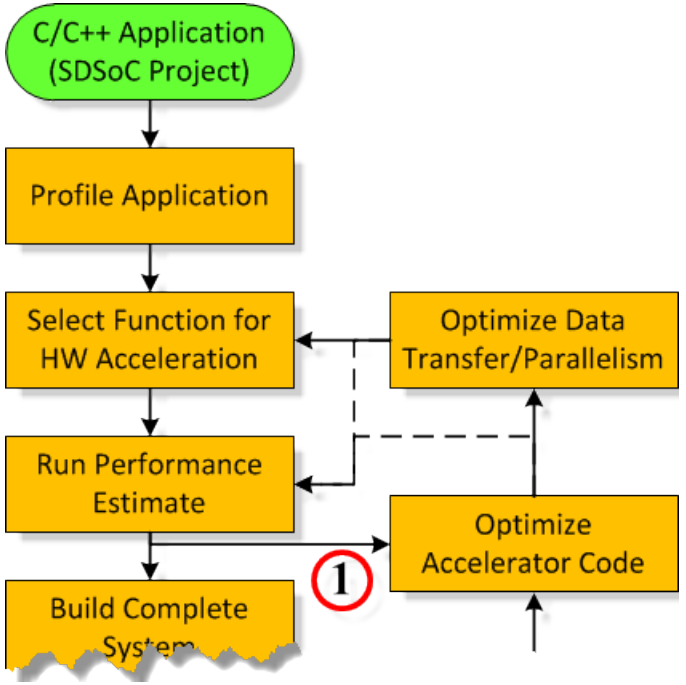
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Estimating Performance

- Enabling the Estimate Performance option builds a project only up to a point that performance estimates can be determined
  - A complete Release or Debug build can take a **long** time
  - The Estimate Performance option shows the impact of moving functions to hardware in only a few minutes
- Comparison of hardware-accelerated system with original software-only system is accomplished by producing two separate sets of data, one for each scenario
  - The Vivado HLS tool is used to produce data for hardware estimates
  - Generated ELF must be run on the actual target to generate data for software estimates
  - IDE provides a Report viewer that compares and illustrates the data

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Initial Development Flow

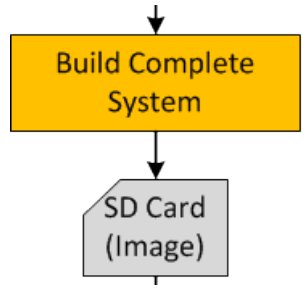


- Building with the Estimate Performance option yields enough information to fine-tune optimization
- First attempts often produce poorer performance than software alone
  - Typical when code has not been refactored and/or annotated for acceleration
- Recommendation: Initial design iterations should use the "short" path until performance improvements are seen
  - Begin by optimizing code to improve accelerator performance, parallelism, and data flow
  - Rebuild to observe impact of changes on estimates
  - Repeat cycle until satisfactory results are achieved
- Detailed system analysis and fine-tuning should be performed next
  - Building and analyzing the full HW/SW system

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Building the Complete System

- Building a project is where SDSoC does all the heavy lifting
  - Three basic methods to run the build process
    - Through the IDE, using a makefile, directly from the command line
  - It is during this step that SDSoC calls upon its internal framework and several sub-executables to accomplish
    - (1) system compilation, (2) system analysis, (3) system generation
- Activate the Release build configuration for a fully optimized build
- A successful build will result in several output products including the following key items
  - Application program in ELF format
  - Bitstream (optional)
  - SD card image (optional)
  - Design projects (e.g. Vivado Design Suite and Vivado HLS tool)



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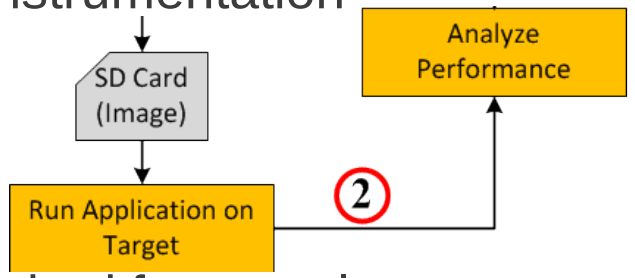
Running the Application

- Standalone applications do not require but can use an SD card
  - When SD card is used, the SSBL in the binary file is replaced by the application ELF
    - Boots directly to the application ELF
  - Applications can be run from the IDE using an SDSoC tool Run configuration
- SDSoC development environment requires use of an SD card to run applications for Linux
  - Files required to run the application on hardware are grouped together as an SD card image
    - First stage bootloader (FSBL), bitstream, and second stage bootloader (SSBL) embedded in a single binary file (BOOT.BIN)
    - Linux kernel
    - Application ELF
    - Other miscellaneous files
  - ELF must be explicitly run from the mounted SD card directory

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Analyzing the Built System

- The goal of this step is to analyze the performance of the updated hardware/software system
- The same tools and techniques used initially apply here: profiling, instrumentation
  - Profiler tool for relative software execution times
  - Time-stamping functions provided through SDSoC API (sds_lib)



- System consists of hardware and software with additional tools required for complete analysis
  - Vivado HLS tool provides reports detailing generated hardware (included with output products)
  - Vivado Design Suite can open the generated system hardware design to review additional reports, modify hardware
  - SDSoC tool compiler can optionally insert an AXI performance monitor (APM) into the generated system
    - APM monitors dataflow between the PS-PL

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Optimizing the System

- Optimizing the system is broken down into two steps: accelerator and then data flow and parallelism
- Optimizing the accelerator consists of refining and/or annotating the hardware function (micro-architecture)
  - Re-factoring code to be more HLS-friendly
  - Adding code annotations (i.e., pragmas) that HLS can interpret and use to better optimize the accelerator
- For system-level optimizations (data-flow/parallelism) there are several options (macro-architecture) including
  - Using physically contiguous memory
  - Using shared memory
  - Using multiple instances of the same hardware
  - Overriding HLS default behavior

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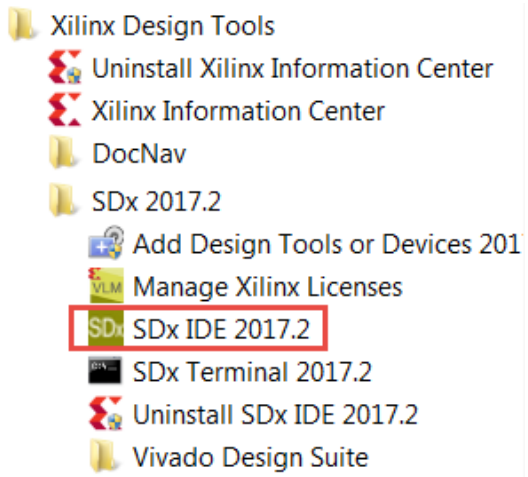
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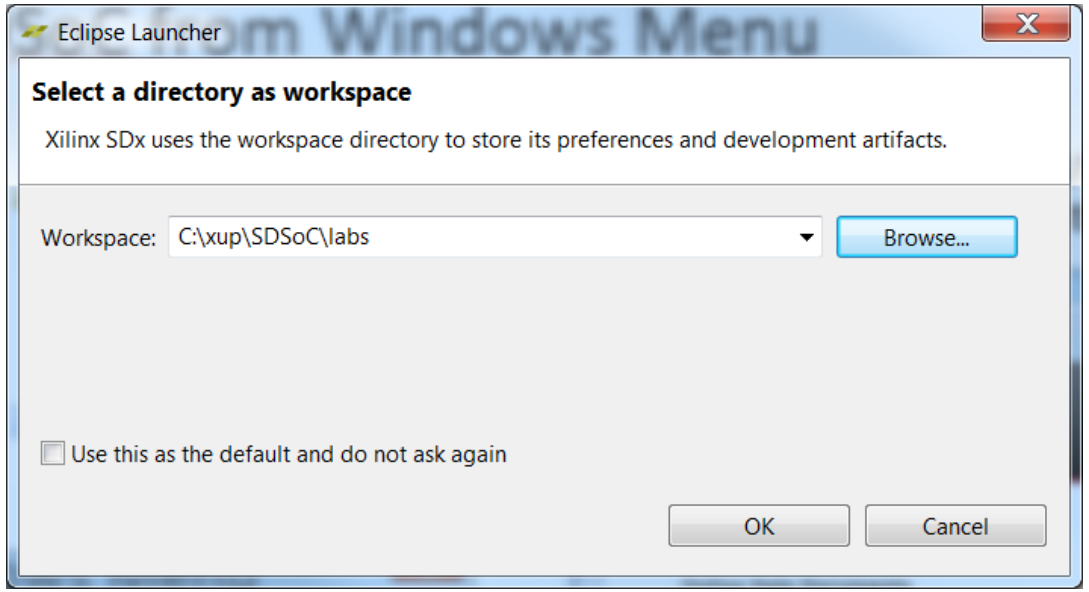
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Invoke SDSoC from Windows Menu

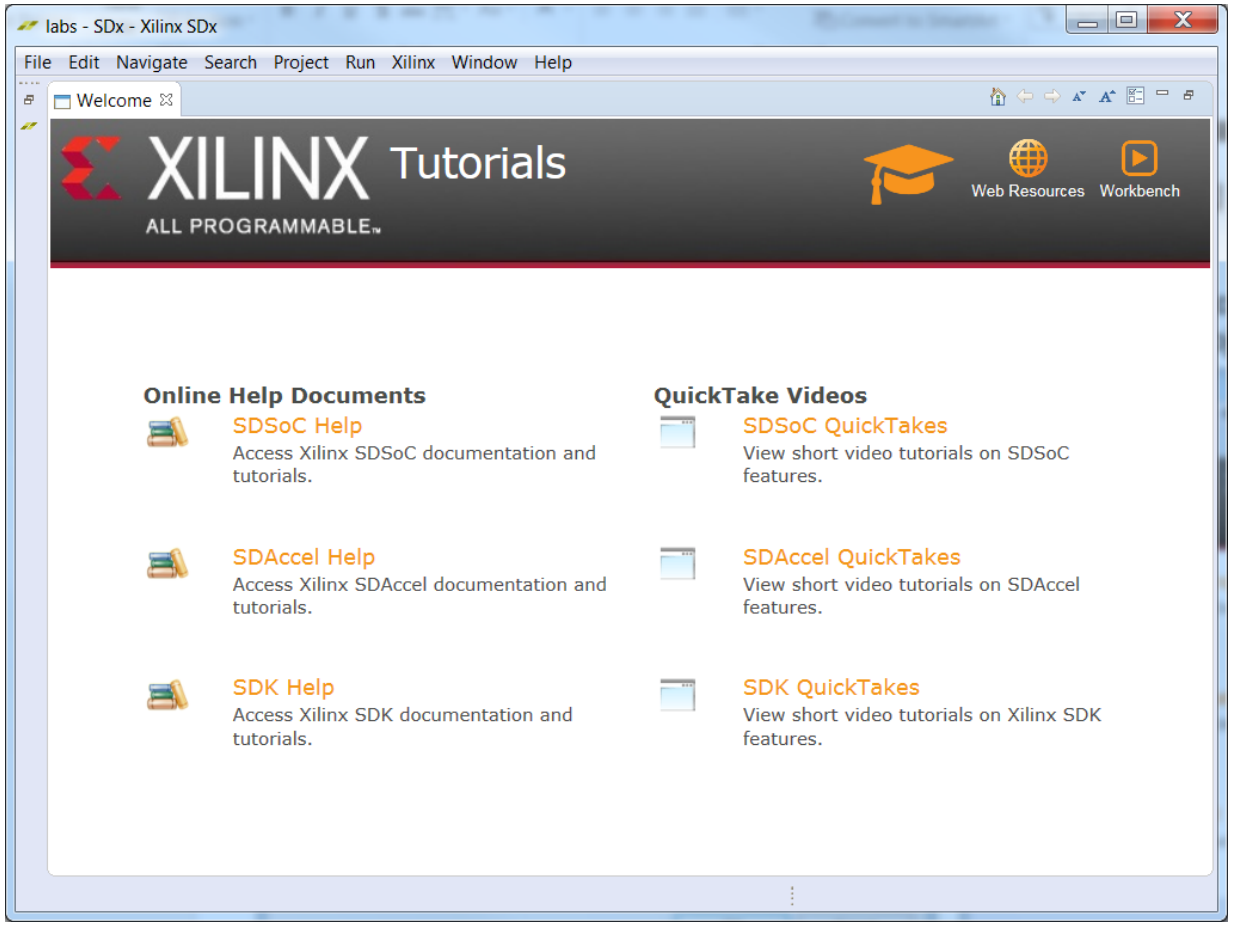
1. Start SDSoC



2. Select a workspace



3. If workspace empty then Welcome screen appears otherwise projects stored in the workspace are displayed



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Creating, Importing, and Opening Projects

- You can create a new project in the selected workspace either by clicking on the **Create SDx Project** link or by selecting **File > New > Xilinx SDx Project**
  - Identify project name
  - Select target platform
  - Select target OS
  - Select either available template or an empty project option
- You can import an existing project
  - Select archive file if the project is in an archived form
  - Identify path if the project is saved in a hierarchical directory structure

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Project Definition

- An SDSoC project is a folder in a workspace that contains all project files and tool metafiles
- SDSoC projects carry some additional properties beyond these general Eclipse-based concepts
  - Associated with a specific SDSoC development environment platform
  - Built for a specific type of operating system (OS)
- Built-in OS support: Linux (default), Standalone (a.k.a bare-metal), and FreeRTOS

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Operating System Support

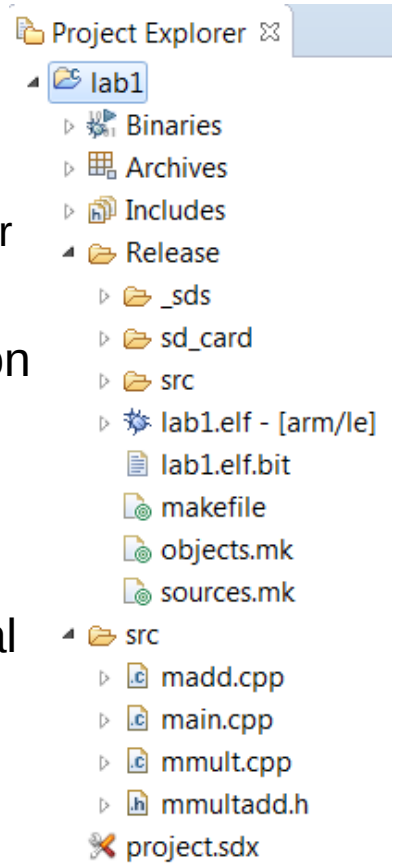
- The output products of an SDSoC project vary depending on the targeted OS
  - For standalone projects
    - *swstubs* folder will include the Xilinx standalone library (*libxil*)
  - For Linux projects
    - SD card image will include a pre-compiled Linux kernel and root file system
    - Pre-compiled kernel contains drivers to communicate with accelerators
  - For FreeRTOS projects
    - Projects will link to a FreeRTOS library supplied by the SDSoC development environment as an extension to the GNU toolchain

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Project Hierarchy

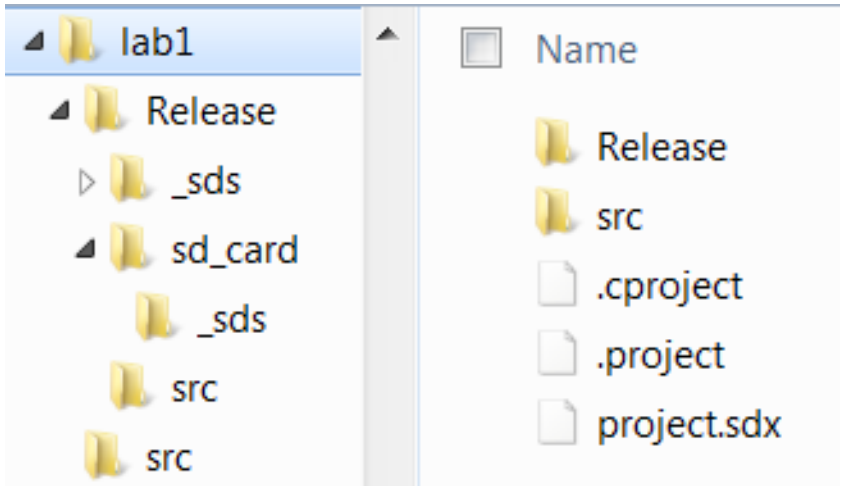
Project Explorer View

- The root folder of a project hierarchy is named after the project itself (*lab1*)
- Three virtual branches are provided: Binaries, Archives, Includes
  - These list executables, libraries, and header files found in or used by the project
- Other branches represent actual folders on the file system: build outputs and source files
- The *src* folder holds source files
- The final element at root level is the actual SDSoC project file: *project.sdx*



Windows Explorer View

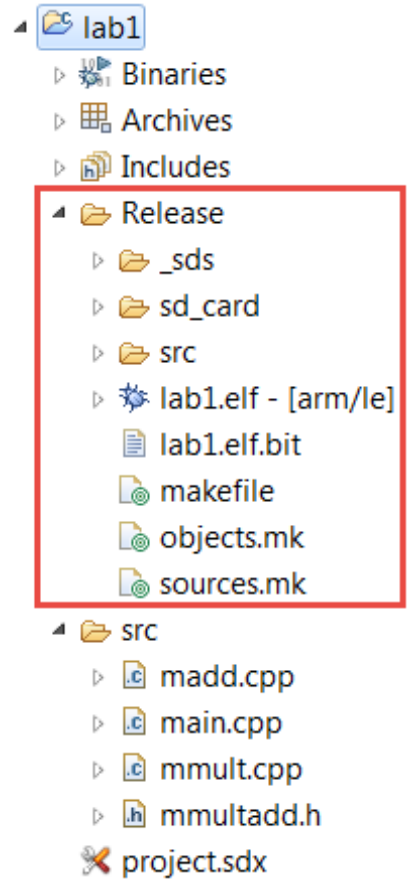
- Hosts real files and directories



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Project Hierarchy (2)

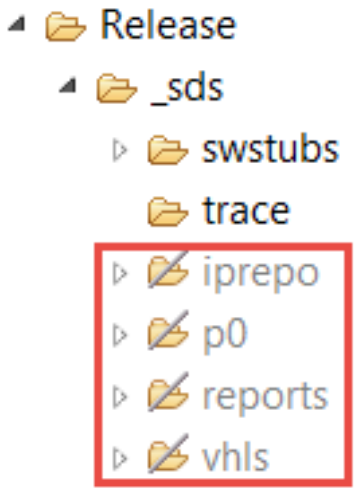
- Common to every build folder are several important components
  - The compiled application executable is placed at the root of the build folder (*lab1.elf*)
  - Several auto-generated make files used by the IDE to initiate the build process
  - The *_sds* folder is a catch all for everything else
    - Reports, files generated by back-end tools (e.g. Vivado Design Suite project), software stubs, etc.
  - An *sd_card* folder that contains the SD card image
    - Not strictly an image but rather a collection of files and folders
  - A *src* folder that contains compiled source files (i.e., object files)



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Project Hierarchy (3)

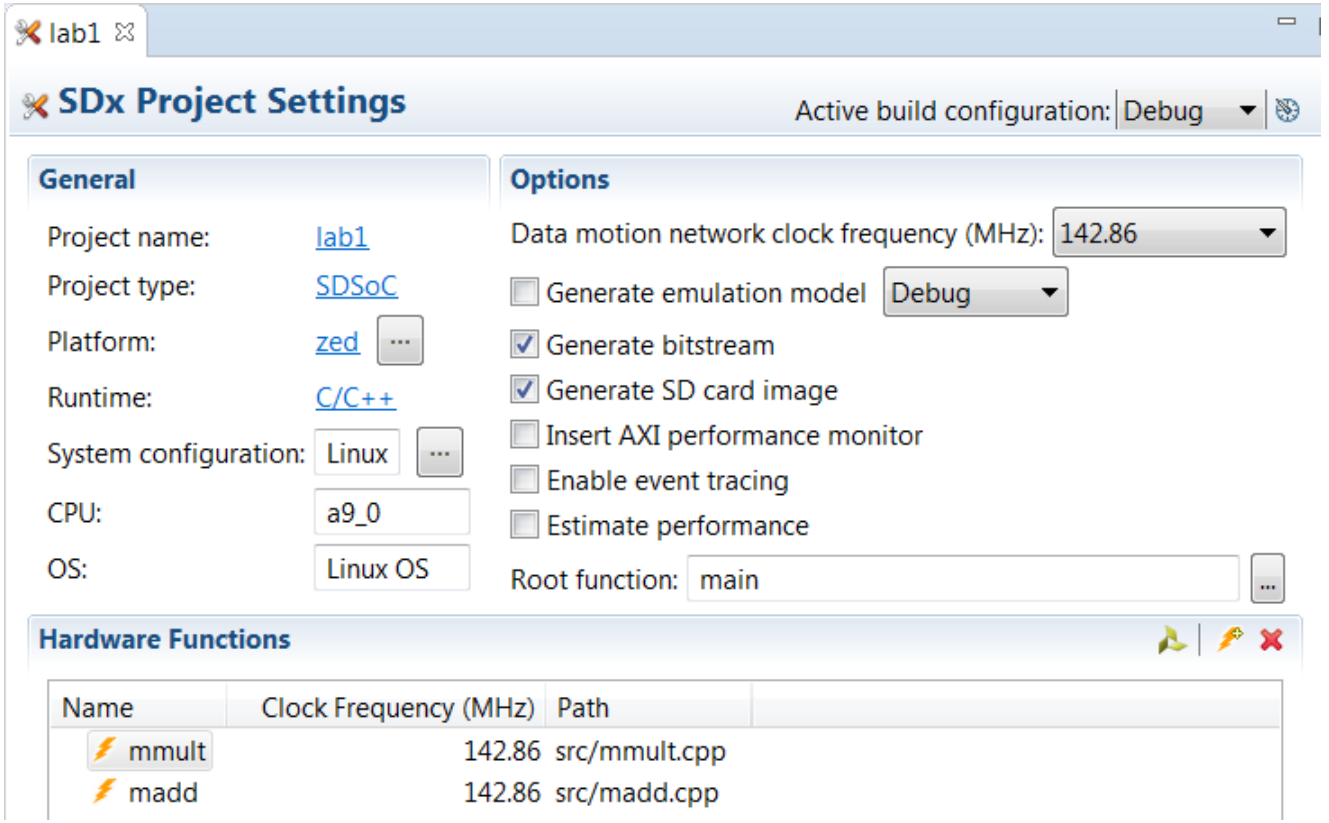
- The *_sds* folder contains several sub-folders
  - *swstubs*
    - Software files and stubs generated and supplied by the SDSoC development environment
    - Some original source code modified to interface with accelerators
  - *iprepo*
    - Repository of cores generated by the Vivado HLS tool (i.e., accelerators)
  - *p0*
    - Vivado IPI project and related files, can invoke Vivado by double-clicking on the *.xpr entry
  - *reports*
    - Various reports including data motion network
  - *vhls*
    - Vivado hls project files for each of the targeted accelerators
- Grayed out folders indicate output products generated by independent back-end tools



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SDx Project Settings View

- Select functions which are hardware target
- Select Data Motion network clock frequency
- Other options



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Summary

- The Zynq-7000 processing platform is a system on a chip (SoC) processor with embedded programmable logic
- The processing system (PS) is the hard silicon dual core consisting of
  - APU and components
    - Two Cortex-A9 processors, NEON co-processor, General interrupt controller, General/watchdog timers
  - I/O peripherals
  - External memory interfaces
- The SDSoC development environment provides a familiar embedded C/C++ application development experience
- Benefits of using SDSoC include
  - Shorter development cycles
  - Simplified interface and partitioning between hardware and software

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